MOS-Gated Thyristors (MCTs) for Repetitive High Power Switching

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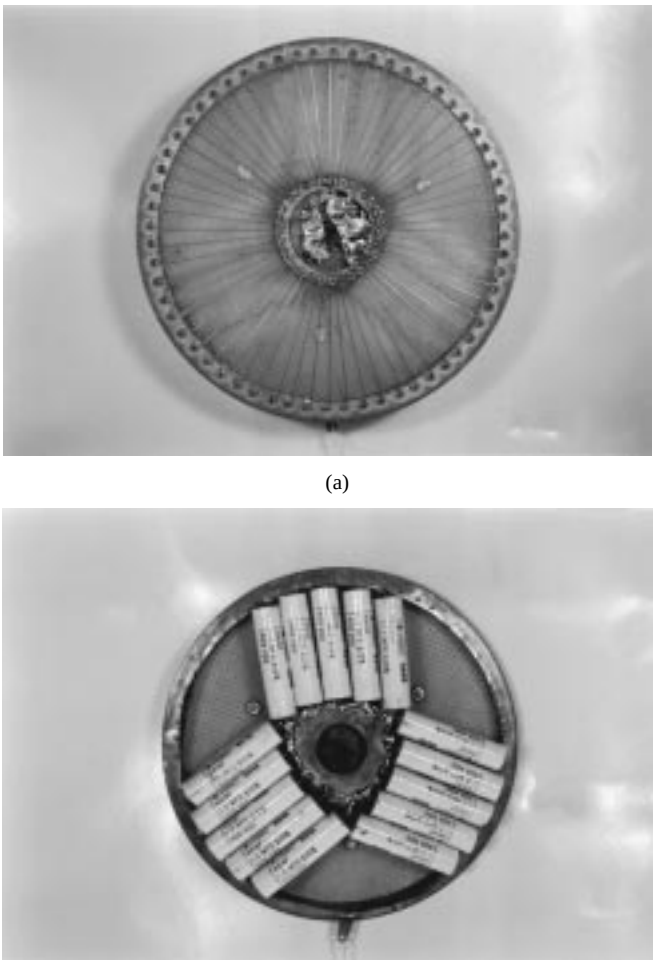
***Abstract*—Certain applications for pulse power require narrow, high current pulses for their implementation. This work was performed to determine if MOS controlled thyristors (MCTs) could be used for these applications. The MCTs were tested as discharge switches in a low inductance circuit delivering 1μs pulses at currents between roughly 3 kA and 11kA, single shot and repetitively at 1, 10, and 50 Hz. Although up to 9000 switching events could be obtained, all the devices failed at some combination of current and repetition rate. Failure was attributed to termperature increases caused by average power dissipated in the thyristor during the switching sequence. A simulation was performed to confirm that the temperature rise was sufficient to account for failure. Considerable heat sinking, and perhaps a better thermal package, would be required before the MCT could be considered for pulse power applications.**

***Index Terms*—High power, power semiconductor switching, reliability, repetitive pulsing.**

I. Introduction

ALTHOUGH power semiconductor switches have been used extensively in many power electronics applications, their utilization in pulse power circuitry has remained low. The principle reason has probably been the perception that short pulse operation, particularly under fast turn-on stress, either was not possible at all, or when possible, led to early failure. However, it has been shown [1]–[5] that high peak currents and fast risetimes can be simultaneously obtained for short pulses in discrete semiconductor thyristors, and that the use of single elements in pulse power circuits is feasible for repetitive peak currents up to 10 kA and di/dt values in excess of 20 kA/μs in the burst mode [5]. Repetitive measurements at a 100 Hz repetition rate have also been successfully performed at around 5 kA and 40 kA/μs [6]. The advantage of thyristors over other types of semiconductor switches is their high blocking voltages and very high surge current capacities. There are, however, several types of thyristors, and both the gate turn-off thyristor (GTO) and the MOS-gated thyristor (MCT) are possible competitors; MCTs have, in fact, been proposed as a superior alternative to conventionally gated SCRs for pulsed power.

Although some comparisons [4] between conventional thyristors and GTOs (and with a thyristor having a GTO geometry [7]) have been made, there have been none with MCTs. This work was done to determine the behavior of MCTs as closing switches (capacitor discharge) under high current, short pulse, and repetitive operation.



(a)

(b)

Fig. 1. (a) Front view of the completed test circuit, which is 17.1 cm (6.75 in) in diameter and (b) back view of the test circuit.

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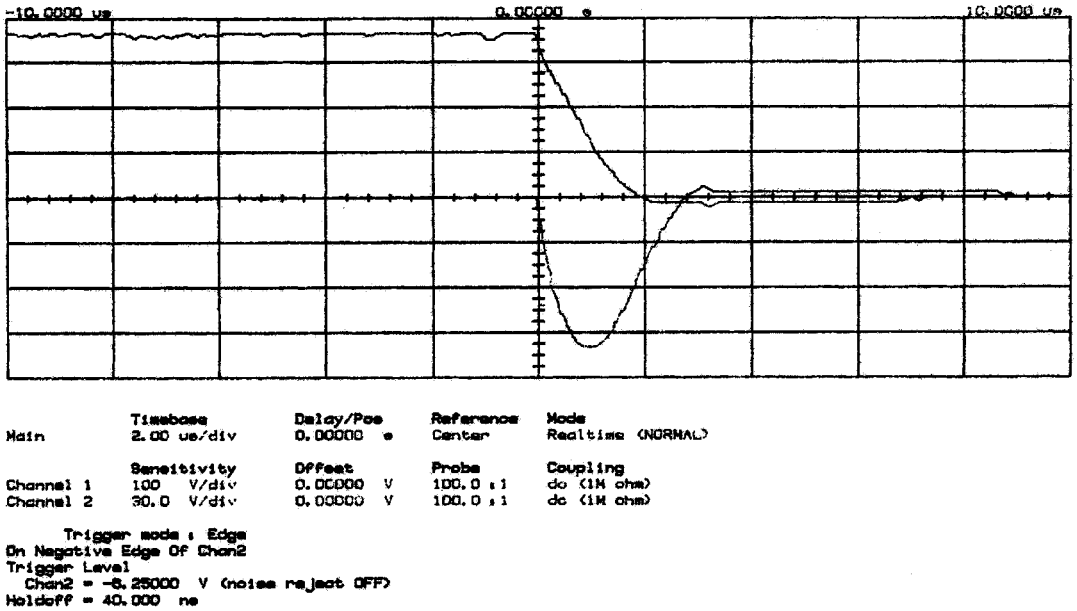


Fig. 2. Voltage and inverted current waveforms for device 2 (these are typical for all the devices tested). The device is switched from 400 V and the peak current is 6800 V. The time scale is 2 μs per large division.

II. Experimental Procedure

A preliminary PSPICE®[1] design was performed of a ring-down test circuit delivering a 1 μs pulse (pulse width at half maximum) at peak currents up to at least 10 kA and pulse repetition rates up to 100 Hz. The design required a total capacitance of 15 μF, discharged into a 25 mΩ load, with a total circuit inductance less than 10 nH. The circuit was implemented in a wagon wheel configuration for the lowest parasitic inductance; Fig. 1(a) (front) and (b) (back) show the front and back sides of the completed circuit. The outside diameter of the complete assembly is 6.75 in (17.1 cm). The load consists of a parallel array of MSW 800 composition wires, isolated from the ground plane by Kapton® insulation, and was measured to be around 24 mΩ. 15. Fifteen 1-μF, 400 VDC ASC capacitors were connected in parallel to obtain the required capacitance. (Although the capacitors were rated only at 400 V, they could be used safely and repetitively, without degradation, up to 600 V.) The device under test is connected in the center of the circuit, where the soldered region is shown, through holes which match the device lead configuration. The circuit was tested by using an MCT itself as a closing switch. Fig. 2 illustrates a typical MCT switched current output pulse waveform (shown inverted); some ringing exists, but is not considered to be significant. The total circuit inductance, based on this waveform, is estimated to be between 5 and 7 nH.

The capacitors were charged using an A.L.E. Systems Model 402L constant power charging supply, and the data were taken with an HP Model 54 502A digitizing oscilloscope. An HP Model 5315B universal counter was used to count the number of pulses before the device failed. Because of the structure of the test circuit, a measurement of the anode current itself could not be performed, but was inferred by measuring the voltage drop (inverted by the oscilloscope) across the load with a Tektronix P-6009 probe. The anode–cathode voltage waveform was measured using another P-6009 probe.

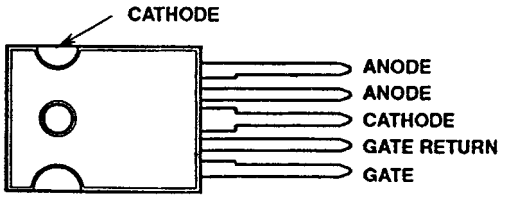
Fourteen commercially purchased Harris Semiconductor 600 V, 75 A p-type MCTs (MCTA75P60) (the MCT technology has now been acquired by SPCO) in the TO-247 package [Fig. 3(a)] were tested as discharge switches both single-shot and repetitively at various voltages between 100 and 600 V and frequencies between 1 Hz and 50 Hz. The total die area for the MCTs is 0.65 cm^2 (0.39 in by 0.26 in), around 62% (0.4 cm^2) of which actively participates in conduction when the device is fully turned on. The cell dimensions are 20 μm on a side, and gating is by way of one turn-on gate per nine cells . Four 0.36 mm (0.015 in) wires are stitch-bonded to the active area [Fig. 3(b)], with conducting surface metal 4 μm to 5 μm thick between the wires. Fig. 3(c) shows a typical device after the packaging epoxy has been stripped off in concentrated boiling sulfuric acid. The external leads did not survive the treatment.

The MCT requires a special gating arrangement, inasmuch as the gate must be driven with a negative voltage relative to its anode, and the driver circuit and the MCT must be isolated from the gating pulse generator (the driver requires an isolated power supply). A noncommercial gate driver and driver circuit board were provided by Harris Semiconductor, and used in these measurements.

III. Experimental Results and Discussion

Every MCT eventually failed when the stress became great enough. Some failed single-shot, some under repetitive stress, but no device could successfully be stressed at a pulse current level higher than around 10 kA. All failure modes were similar, independent of the current level or the pulse repetition rate;

[1]Certain commercial products or materials have been identified in order to specify or describe the subject matter of this paper adequately. In no case does this identification imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the products or materials are best for the purpose.



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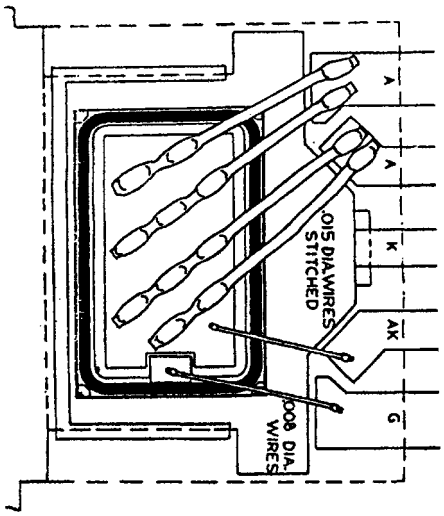

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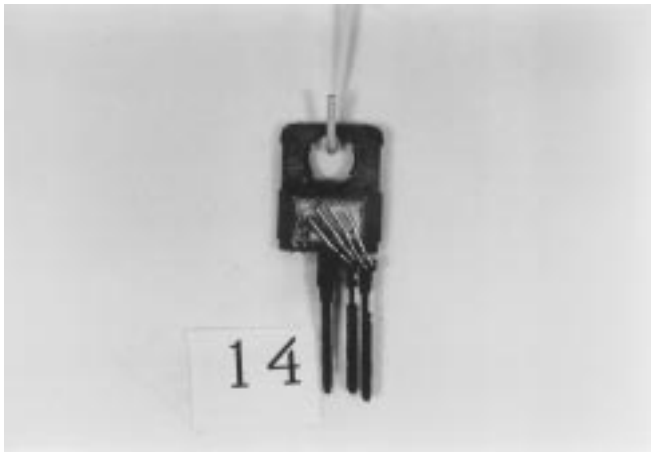

(c)

Fig. 3. (a) TO-247 five lead package. The overall dimension, from the tip of the leads to the top of the package is 1.5 in (3.8 cm), and the dimension of the epoxy packaging is 0.81 × 0.62 in (2.1 × 1.6 cm). The thickness of the epoxy package is 0.185 in (4.7 cm). (b) Internal lead arrangement for the MCT. (c) Representative view of a device (number 4) after the epoxy package has been stripped. The two heavy outermost leads on the right are connected to an anode pin; the two adjacent heavy wires are connected to a second anode pin (these were tied together during the measurement); the outermost light wire on the left is the gate connection; and the inner light wire on the left is connected to the anode as the gate return. The cathode pin is connected to the metal backing, and can be seen as the longest pin in the center of the package.

every anode failed open or resistive, and with only two exceptions, with accompanying failure or degradation of the gate.

The results of the single-shot measurements are shown in Tables I and II. (In these tables, a single shot is defined such that at least 1 s elapsed between one shot and the next.) Device 4 was defective and could not be included in the measurements. Although the number of samples in Table I is relatively small,

TABLE I
TOTAL SINGLE SHOTS AT FAILURE (LOWER CURRENTS WERE OBTAINED AT REDUCED CHARGE VOLTAGE)

Device No.	Peak Current at Failure (KA)	Shots	Comments
1	10.4	5	
5	10.4	5	
3	9.4	2	
7	7.3	100	Did not fail
9	6.8	100	Did not fail
8	3.6	100	Did not fail
6	2.6	3	
2	2.6	1	
4			Defective

TABLE II
TOTAL SINGLE SHOTS AT FAILURE (LOWER CURRENTS WERE OBTAINED AT REDUCED CHARGE VOLTAGE)

Device No.	Shots	1/2 I^2t (Amp^{2}sec)	Peak Current at Failure
1	5	54.8	10.4
5	5	54.8	10.4
3	2	44.2	9.4
7	100	26.6	7.3 (Did not fail)
9	100	23.1	6.8 (Did not fail)
8	100	6.5	3.6 (Did not fail)
2	1	3.4	2.6
6	3	3.4	2.6

the results shown are suggestive. In general, as the current decreased, the survival rate of the devices increases as the current decreases. Devices 2 and 6, which failed rapidly at the lowest current, are exceptions to the trend, and will be discussed below.

Table II is the same as Table I, except that the number of shots to failure is now considered in terms of I^2_{peak}t, the action, I_{peak} being the peak current and t being 1 μs. $I^2_{peak}t$ normally describes the short-time thermal capacity of a thyristor and is used in selecting a fuse to protect the device against a sinusoidal overcurrent surge; it is derived from the total energy dissipated in the thyristor during a surge, $\int I^2R\,dt$. The reduced integral, $\int I^2\,dt$, is the same for all the elements of a series circuit, so that 1/2 $I^2_{peak}t$ is considered appropriate for fusing. In these measurements, however, each device is tested independently, so the series argument cannot be used. However, the devices have the same structure, so that if it assumed that each device is completely turned on, the resistance in the on-state will be similar,

and inasmuch as the pulse shape is roughly sinusoidal, a 1/2 $I_{peak}^2 t$ comparison is not entirely inappropriate and can be instructive. It should be pointed out that the assumption of complete turn-on may not be met in every case; in this event, the thermal stress caused by heat dissipation will be even greater. This point will be considered further in the discussions of Devices 2 and 6. Ignoring Devices 2 and 6 for the moment, Table II indicates more clearly that high current stress, which increases with the square of the current, is a likely reason for the failure of the devices, and that the early single-shot failure of devices 1, 5, and 3 is probably the result of thermal effects. The thermal stress for devices 7, 9, and 8 is evidently not great enough to cause failure under single-shot conditions, even at 100 shots.

Respecting Devices 2 and 6, it is possible to speculate on the reason for the failure at a low number of shots. The active region of these MCTs is an epitaxial layer 100 μm thick. In full turn-on, the entire epitaxial region is conductivity modulated, so that power dissipation in the device is at a minimum, and if the modulation is incomplete at the maximum current, the dissipated power is correspondingly higher. The plasma spreading velocity is a function of current density [8], [9]; using values estimated on the basis of the relationships described in these latter references, at 0.5 μs, where the current peaks, the plasma depth varies from approximately 150 μm at 10.4 kA to 100 μm at 3.6 kA. However, at 2.6 kA, the peak currents for Devices 2 and 6, the plasma depth is only about 90 μm. In this case, dissipation would be high even at reduced peak current, and early one-shot failure could occur. This analysis is not intended to be a conclusive argument, but it is suggestive. In every case, the current flow would probably be homogeneous across the active area although only one in nine cells were triggered on because the plasma spreading velocity, even at the lowest peak currents, is high enough so that lateral plasma spreading would not be an issue.

The results of the repetitive measurements are tabulated in Tables III and IV. The values of the peak current were chosen from Table II to be in the optimum range for survival at repetitive stress. Although the heating in individual pulses is adiabatic, repetitive pulsing will cause an average temperature buildup which causes considerably more stress than a single shot, or a series of single shots. Furthermore, a history of prior multi-single-shot stress, may predispose a device to earlier repetitive failure This may be the case for Devices 7, 9, and 8, which had previously been stressed single-shot first 100 times, and particularly for Device 8, which had been single shot-stressed at the current border for incomplete plasma filling. Of the others, Device 12 was first tested single-shot, then at 10 Hz; devices 11 and 14 were tested single-shot and then at 50 Hz; device 13 was tested single-shot, at 10 Hz, then 50 Hz; and device 10 was tested single-shot, and at 1, 5, 10 and 50 Hz to failure. Although 1/2 $I_{peak}^2 t$ was the same for Devices 12. Eleven and 10 (Table IV), Device 12 underwent almost four times as many pulses before failure as Device 11, and ten times as many as Device 10. This is probably attributable to the lower pulse repetition frequency for Device 12, so that the cumulative temperature increased more slowly. Device 13 was also tested at 50 Hz, but did not fail as soon as Devices 11 and 10. In this case, 1/2 $I_{peak}^2 t$ was lower for Device 13. The failure in Device 14 appears anomolous.

TABLE III
TOTAL REPETITIVE SHOTS AT FAILURE (LOWER CURRENTS WERE OBTAINED AT REDUCED CHARGE VOLTAGE)

Device No.	Peak Current at Failure (KA)	Shots	Highest Frequency at Failure (Hz)
12	6.8	9000	10
11	6.8	2750	50
10	6.8	1000	50
9	6.8	6	1
13	5.2	4505	50
14	5.2	55	50
7	4.7	450	10
8	Failed Immediately	1	1

To eliminate the possibility that thermal failure might have occurred in the very thin metallization between the lead wire bonds, the epoxy packaging material was stripped and the surfaces of the devices examined microscopically, no damage, in general, could be seen. Table V lists the results of the examination performed by Harris Semiconductor. Inasmuch as no metallization failure was observed, failure caused by the instantaneous high power densities, and the evolution of high junction temperatures occurring during repetitive switching, was reconsidered as a failure mode, and thermal calculations were performed. (Gate failure is probably a corollary of the junction failure, and was not considered a primary mode.)

The power and energy delivered per pulse were calculated for a device tested at 400 V and a peak current of around 7 kA, pulsed repetitively at 50 Hz. The power pulse was obtained simply by a point-by-point in time multiplication of the voltage across the MCT and current flowing through it at that time, and the energy per pulse was found by numerically integrating the power over time. Fig. 4 is a plot of power and energy delivered to the device per pulse. An analytical pulse-by-pulse calculation of the temperature increase in the device was not practical, so a numerical simulation was performed using the silicon chip and TO-220 package thermal models provided in Saber® [8], [9]. Heat generation was assumed to occur over the entire thickness of the device (0.036 cm) and the effective area for conduction (0.4 cm^2). The silicon chip thermal model assumes that the specific heat of the silicon remains constant during the pulse sequence, but the thermal resistance of the silicon varies with temperature. This approximation is reasonable within the temperature range used in the simulation, the intrinsic temperature of the silicon (480K), which was considered to be the failure temperature.

Fig. 5 illustrates the power and energy per pulse used in the simulation to represent the measured power function of Fig. 5. Although the power pulse used for the simulation (shifted in time by 1.0 ms) differs in its shape, the simulated energy deliv-

TABLE IV
TOTAL REPETITIVE SHOTS AT FAILURE (LOWER CURRENTS WERE OBTAINED AT REDUCED CHARGE VOLTAGE)

Device No.	Shots	Peak Current at Failure	1/2 I^2t (Amp^{2}sec)	Highest Frequency at Failure
12	9000	6.8	23.1	10
11	2750	6.8	23.1	50
10	1000	6.8	23.1	50
9	6	6.8	23.1	1
13	4505	5.2	13.5	50
14	55	5.2	13.5	50
7	450	4.7	11.1	10

TABLE V
RESULTS OF MICROSCOPIC EXAMINATION

Device No	Comment
1	No sign of failure; cells were sharply defined even at 160X
2	Epoxy was not fully removed, but the cells which were visible next to the power leads appeared to be undamaged; no sign of failure
3-5	Same as Device 2
6	Same as Device 2, although epoxy removal is not as good
7-8	Same as Device 2
9	Excellent epoxy removal; no signs of failure
10	Die cracked across entire width. This was believed to have occurred during shipping.
11-14	Same as Device 2

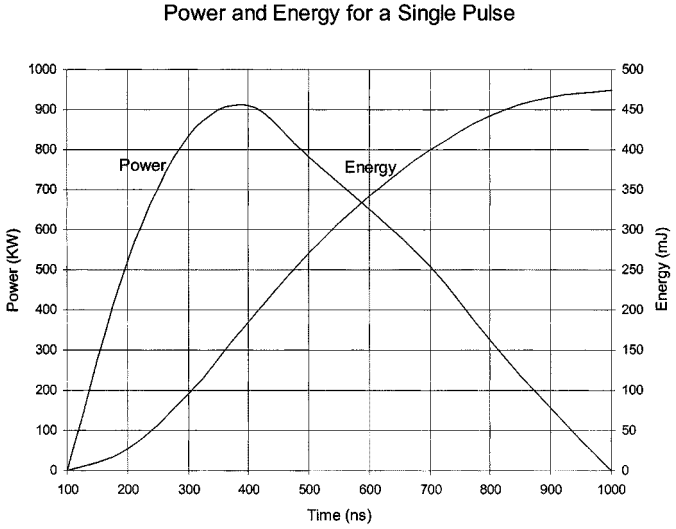

Fig. 4. Plot of the power and energy for a single pulse (device number 2).

ered to the device, which determines the temperature increase, agrees well with that of the actual pulse.

Two simulations were performed, one assuming that no heat sinking other than the cathode tab was involved (the conditions of the actual experiment), and the other assuming that heat sinking was enhanced. Both simulations were performed at 50 Hz over the same time scale and are shown in Fig. 6. The top of the envelope of each curve represents the peak temperature of the junction just after a pulse has been delivered, and the bottom envelope temperature is its value after cooling, just before the next pulse arrives. Both temperatures increase with time; however, failure occurs when the bottom temperature equals the intrinsic temperature. In the case of enhanced heat sinking, the device does not fail after 100 s, or 5000 pulses. In the case of no additional heat sinking (lower curve), the device fails at around 10 s, or 500 pulses. Heak-sinking effect is evidently present in the actual measurements, inasmuch as several thousand pulses were obtained even at the higher currents, but a possible explanation for the earlier failures is perhaps incomplete turn-on and greater heat evolution.

IV. CONCLUSION

Although the total number of measurements is not large enough for a complete statistical analysis, the results nevertheless strongly suggest that excessive heat dissipation is responsible for failure in MCTs at short pulses and high currents. At lower peak currents, the $I^2_{peak}t$ losses themselves may not be sufficient for burn-out, but if complete plasma filling in the epitaxial region is incomplete, as can be argued, thermal losses may still be great enough to account for the failures.

The results are similar for repetitive measurements at intermediate currents, and appear to be related to increasing thermal buildup with increasing frequency. The theoretical results show that the peak temperature rises sufficiently after a sufficient

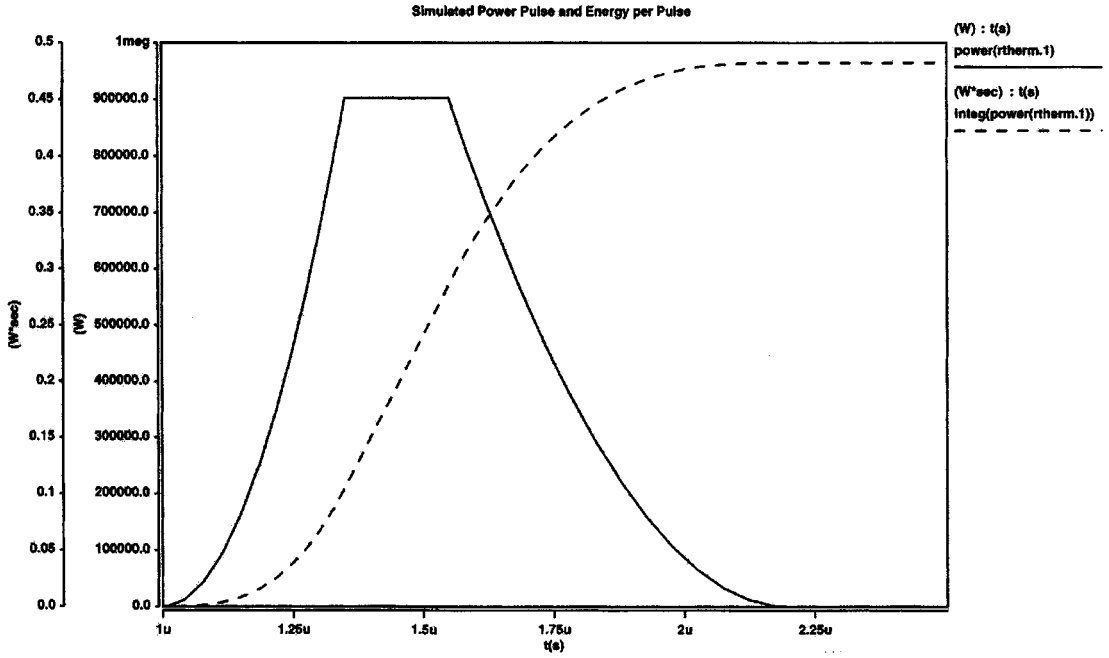

Fig. 5. Simulated power per pulse and energy per pulse, and used in the thermal simulation.

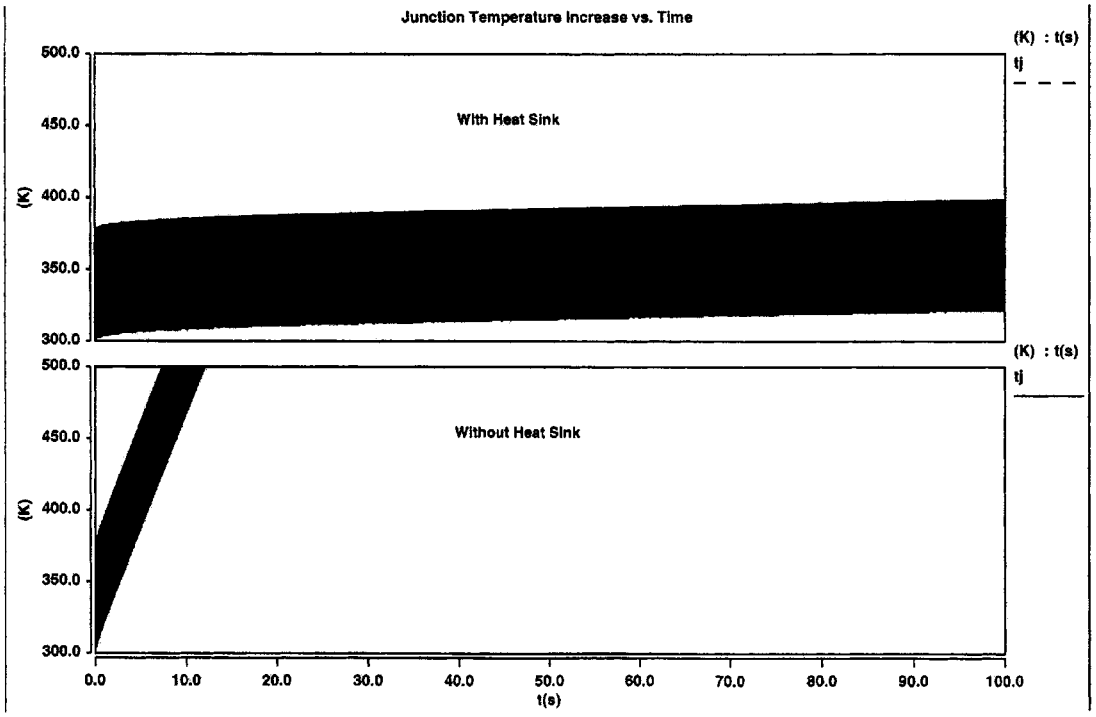

Fig. 6. Results of simulation of temperature excursions in the MCT with enhanced heat sinking (upper curve) and with no additional heat sinking (lower curve).

number of pulses to drive the epitaxial material intrinsic, with thermal runaway likely to follow. It was not possible, under the conditions of the experiment, to provide more extensive heat sinking, which would perhaps have adequately confirmed this theoretical conclusion. Even with heat sinking or a better high temperature package, however, it is unlikely that, at this time, a sufficient number of pulses at repetitive operation can be obtained to allow these MCTs to be used reliability as an applications switch.

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