AC Josephson Voltage Standard: Progress Report

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Abstract—Progress toward a Josephson voltage standard for fast dc measurements and accurate ac waveform synthesis is described. A superconductor-normal-superconductor (SNS) junction process is used to make 5 mA critical current arrays with up to 32 768 junctions. With rf excitation at 11 GHz these arrays generate milliampere constant-voltage steps. A bias control circuit that provides output current amplification, transient suppression, and submicrosecond settling time is used with both superconductor-insulator-superconductor (SIS) and SNS junction arrays for fast, automated measurements of A/D converter linearity, a test for subnanovolt accuracy, waveform synthesis, and a preliminary measurement of the ac-dc difference of a thermal voltage converter.

Index Terms—AC, digital-to-analog converter, Josephson, standard, voltage, waveform synthesis.

I. INTRODUCTION

THIS PAPER describes a Josephson voltage standard (JVS) in which the output voltage $V = Nf/K_J$ is defined by digitally programming the step number N. In a programmable JVS, an array of nonhysteretic junctions is divided into a binary sequence of array segments as shown in Fig. 1. The microwave excitation for each junction is set to equalize the amplitude of the $n = 0$ and $n = 1$ steps as shown in the inset. Each segment of the array can be set to the $n = -1, 0$, or $+1$ step by applying a bias current $(-I_s, 0, +I_s)$ at the appropriate nodes. The combined step number N for the whole array can thus be set to any integer value between $-M$ and $+M$, where M is the total number of junctions in the array [1].

The rapid settling time and inherent step stability of the JVS in Fig. 1 make it potentially superior to a conventional JVS for dc measurements. (We define a dc measurement to be one in which the transient associated with changing N can be excluded from the measurement.) Such measurements include calibration of dc reference standards and digital voltmeters, and the characterization of A/D and D/A converters. The circuit of Fig. 1 can also be used to generate a staircase approximation to a sine wave by selecting appropriate step numbers in rapid succession. In theory, the resulting waveform has a computable rms value and might be used to confirm the ac-dc difference of a thermal voltage converter and for other ac measurements. In the case of ac measurements, however, the transient waveform during step transitions is included in the rms value and may lead to an unacceptably large uncertainty. Practical measurements may also require an output current of several milliamperes—well beyond the current sourcing
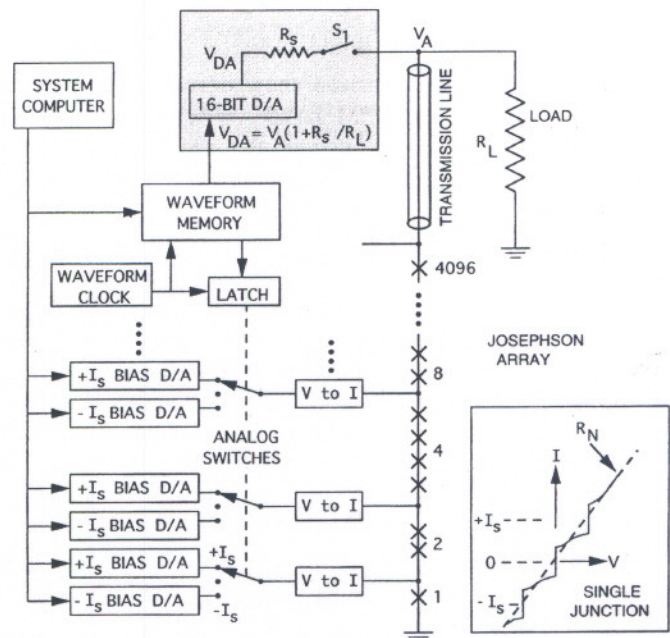
Fig. 1. An automated bias system for a programmable Josephson voltage standard.

capability of a typical Josephson array. These problems are resolved by an addition to the bias circuit that can amplify the output current and minimize transients at the step transitions as shown in the shaded portion of Fig. 1.

II. BIAS-CIRCUIT DESIGN

The bias circuit of Fig. 1 has been developed for evaluating and optimizing the performance of programmable Josephson arrays with up to 24 segments. Under the control of the system computer it can individually measure the *I-V* curve of each array segment to confirm functionality and to select the optimum bias points for the -1 and $+1$ steps. With the optimum bias current values latched into the D/A converters, any specified dc value Nf/K_J is generated by setting the analog switches to bias the appropriate array segments into the $+1, 0$, or -1 states. To synthesize an ac waveform, the computer loads the waveform memory with the required state $(-1, 0, +1)$ of each array segment for up to 65 536 time steps of the specified waveform. When the waveform clock is started, the memory steps through the time sequence and its outputs drive the analog switches that select the bias appropriate to the $-1, 0$, or $+1$ steps for each array segment. The outputs of the analog switches control fast constant-current drivers for the array bias lines. A latch on the digital inputs to the analog switches ensures that all switches change
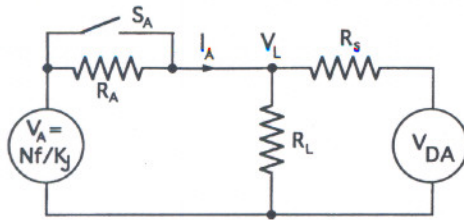
Fig. 2. An equivalent circuit for the array bias circuit.

6 Active Bits

12 Active Bits

Fig. 3. Low frequency sinewaves synthesized with 6 and 12 bits of a programmable Josephson array.

state within a few nanoseconds. The settling time of the bias current drivers is 400 ns.

The voltage across the Josephson array is accurately controlled only if the bias point for each junction remains within the bounds of the constant voltage step. Thus the load current is limited to about half of the step width, or about 10 μA to 1000 μA, depending on the junction technology used. This output current may be inadequate for applications such as the measurement of the ac/dc difference of thermal voltage converters. When switch S_1 is closed, the 16-bit D/A converter in the shaded portion of Fig. 1 can provide a substantial amplification of the available output current. This increased output capacity results because the D/A converter is programmed to provide the predicted load current and the Josephson array need only supply the difference from the predicted value. If the prediction is accurate to 1%, then the circuit can multiply the available output current by a factor of 100.

If R_s is of order 1 Ω to 10 Ω, then the shaded circuit will also suppress the transients that occur when the Josephson array switches between steps. Consider the transition from $N = 127$ to $N = 128$. In this case six array segments with a total of 127 junctions will make a transition from 1 to 0 and one segment with 128 junctions will make a transition from 0 to 1. For the worst case timing error with S_1 open, the voltage during the transition could be as small as 0 or as large as 255 f/K_J. With S_1 closed, the array bias circuit can be represented by Fig. 2. Here, the array and its segment bias currents are approximated by a voltage source of value $N f/K_J$ in series with a resistance R_A that is shunted by switch S_A. R_A is the dynamic resistance of the array for currents outside the range of the constant voltage steps (see Fig. 1 inset). Typically $R_A \approx MR_N = 1$ kΩ to 10 kΩ where R_N is the normal state resistance of a single junction. The I-V curve of the array is approximated by specifying that switch S_A closes for bias currents within the range of the step. During the transient, S_A is open and the sensitivity of the load voltage to the array transient is given by

$$dV_L/dV_A = (R_s R_L)/(R_s R_L + R_A R_s + R_A R_L). \quad (1)$$

For typical values $R_A = 1$ kΩ, $R_L = 1$ kΩ, $R_s = 1$ Ω, the sensitivity is $dV_L/dV_A = 0.001$. The transient in the array voltage is thus attenuated by a factor of 1000. As the transient dies out, I_A will fall within the step range (S_A closes) and V_L settles to exactly V_A. Thus the load voltage is controlled by the array between transitions and by the 16-bit D/A during transitions. State-of-the-art 16-bit D/A converters are capable of reducing the transient to about $\Phi = 60$ pV · s. Assuming the worst case in which all of the transient errors add constructively, the resulting rms error in a 1 V, 60 Hz
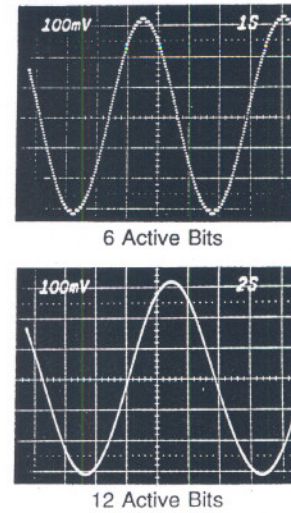
sine wave approximation with 256 transitions would be about 1 part in 10^6.

III. JUNCTION DESIGN

Experimental realization of the programmable JVS has been pursued with both superconductor-insulator-superconductor (SIS) and superconductor-normal-metal-superconductor (SNS) junctions. In the case of SIS junctions, the required nonhysteretic I-V curve is achieved by adding a shunt resistor in parallel with each junction. Theoretical analyzes [2]–[4] have shown that the best combination of bias margin, stability, and microwave drive power is achieved when the step voltage f/K_J is approximately equal to $I_c R$ where I_c is the junction critical current and R is the shunt resistor. In practice, the shunt resistor has an unavoidable parasitic inductance on the order of 1 pH. The resistor is effective only if its inductive reactance at the drive frequency f is small compared to its resistance. Thus for practical frequencies, $f < 100$ GHz, the maximum critical current is about 300 μA. The shunt resistor for SNS junctions is inherent to the metallic barrier, and its inductance is negligible. In this case, I_c is only limited by the available microwave power and/or heating effects, and step amplitudes of several milliamperes are easily achieved. Large critical currents are essential to achieve the noise immunity that high speed operation demands. For this reason, the SNS junction geometry is now the preferred design for programmable voltage standards.

IV. EXPERIMENTAL RESULTS—SIS JUNCTIONS

A tapped array of 8192 shunted SIS junctions has been fabricated. It is designed to operate at 75 GHz and generate voltages from −1.2 V to +1.2 V with 14 bits of resolution. Flaws in the largest array segments have limited its range of operation to −0.3 V to 0.3 V. This device has been used in a number of experiments to prove the utility of programmable Josephson arrays. In the first of these experiments a much slower predecessor to the bias system described above was used to synthesize a very low frequency sine wave. Fig. 3
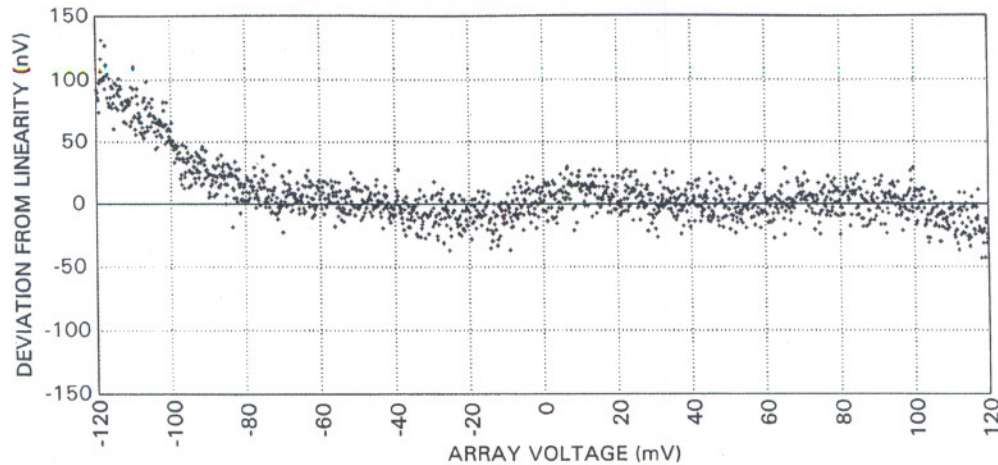
Fig. 4.   Linearity deviation of a DVM as measured by an 8192 junction programmable Josephson array.
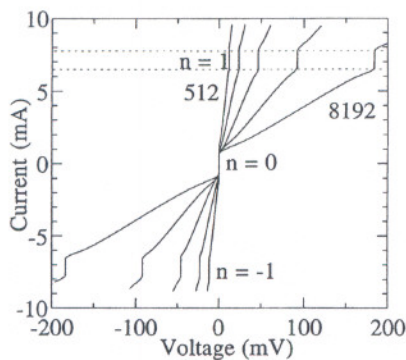

Fig. 5.   *I-V* curves for 512, 1024, 2048, 4096, and all 8192 junctions of a SNS array.

shows the 600 mV peak-to-peak step approximations using 6 and 12 bits of resolution. Although Fig. 3 is a nice picture, the waveforms are not in the realm of metrological accuracy because too great a portion of the waveform occurs during the uncontrolled transitions between steps.

This experiment underscored the necessity of developing the fast, parallel, transient-suppressed bias system described above. In order for the fast bias system to be effective, all of the bias leads to the chip must have a bandwidth of several megahertz. Unfortunately, the room temperature noise delivered to the chip through this wide bandwidth washes out the relatively small ($\sim$50 μA) steps that are typically achieved with SIS junctions. Thus, in addition to the fast bias system, arrays that generate much larger steps are required.

Since programmable Josephson arrays do not operate at zero bias current, there is a very real possibility that a small series resistance will add an unknown, bias dependent, offset voltage. To test for this error we performed an experiment in which 1024 junctions are switched between having all junctions in the 0 state, to having half the junctions in the +1 state and half in the −1 state. If the difference in array voltage between these two bias conditions remains zero over a range of bias current, then there is very strong evidence that all junctions are generating the correct voltage and that there is no anomalous offset voltage. In one such experiment, the measurements were averaged for several hours, and we found

a difference voltage of 0.1 nV with an uncertainty of 0.3 nV. In a similar experiment we synthesized a 400 Hz square wave and confirmed that its rms value remains constant over a 30 μA range of junction bias currents. The automated setup procedure for all of our measurements now checks that the steps are flat to better than 100 nV.

In the last experiment with SIS arrays we applied the array voltage to a DVM and compared the DVM reading to the computed array voltage on every step from $N = -750$ to $N = +750$. Fig. 4 is a plot of the linearity deviation of the DVM relative to the array for the 1500 data points. The ability to digitally select the array step voltage and to be certain that there will be no spontaneous transitions between steps makes this measurement much faster and simpler than would be the case using a traditional hysteretic Josephson array.

V. EXPERIMENTAL RESULTS—SNS JUNCTIONS

SNS junctions are intrinsically shunted by the conductivity of the metallic barrier. The junctions that we are using have a palladium-gold barrier for which the $I_c R_N$ product is typically 5 μV to 20 μV [5]. Using the condition that $f/K_J \approx I_c R$ as described above leads to an optimum drive frequency near 8 GHz. The arrays work nearly as well at frequencies up to 15 GHz so we use this higher frequency to increase the output voltage range. Since the resolution of this type of Josephson standard is given by the step separation, the lower frequency relative to the SIS design results in higher resolution at the expense of requiring more junctions per volt of output range. (At 15 GHz, 32 240 junctions are required for 1 V.) Fortunately the SNS junction process is able to generate large arrays of highly uniform 2.5 μm diameter junctions with critical currents near 5 mA [5]. With such high critical current density (100 000 A/cm^2) and the corresponding high bias currents, we have encountered difficulty with breakdown of wiring contacts in the circuit. Also, for $I_c > 5$ mA, the rf power dissipated in each junction ($P \approx I_c f/K_J$) leads to excessive chip heating for very large arrays [3]. Fig. 5 shows *I-V* curves of the segments 512, 1024, 2048, 4096, and all 8192 junctions of an 8-segment SNS junction array operated at 11 GHz. (The maximum voltage is 186 mV.)

The $n = -1, 0$, and $+1$ steps are all larger than 1 mA and occur over identical bias current ranges for every segment. This precise matching of the *I-V* curves of thousands of junctions is one of the critical requirements of a programmable array.

The junctions are arranged in series along the center conductor of a 50 Ω coplanar waveguide. In contrast to the 3 Ω striplines used in the SIS design, the coplanar design eliminates two fabrication levels. Also, because of the larger ratio of line impedance to junction resistance, it is possible to maintain the required rf power uniformity through a larger number of junctions. The lower frequency used in the SNS design makes the rf dividing network too large to fit on the chip, so most of the divider network is on the finger contact board to which the chip mounts. Typically 4096 junctions are used in each branch of the rf distribution network.

A 32 768 junction SNS array designed to reach 1 V is under development. An important goal of this circuit is the direct measurement of the ac-dc difference of a thermal voltage converter (TVC). Since the array can be programmed to generate either ac or dc, this measurement can be made without switching between sources. A variety of difficulties including junction yield, flux trapping, and circuit contact breakdown has limited these measurements to an array of 4096 junctions operating at 13.2 GHz to generate a maximum voltage near 0.1 V. The transient suppression circuit of Fig. 1 is designed to minimize transients at the load, but, because of delay and mismatch in the transmission line to the Josephson array, this circuit can generate flux trapping current spikes at the array. Since our present devices are susceptible to flux trapping, it was necessary to disconnect the transient suppression circuit and to increase the bias current risetime. In the best result to date we compared the output of a 100 Ω multijunction thermal converter (E_{ac} or E_{dc}) for a 112 mV dc input, a -112 mV dc input and a ±112 mV, 50 Hz square wave input. We compute E_{dc} as the average of the $+$dc and $-$dc measurements that are symmetrically positioned around an ac measurement. This particular TVC generates only about 96 μV for a 112 mV input so 387 measurements were averaged to obtain a small uncertainty for the ac-dc difference. Assuming a square law response ($n = 2$) we find the ac-dc difference $\delta = (E_{dc} - E_{ac})/nE_{dc} = 18 \times 10^{-6}$ with a standard deviation of the mean of $\pm2 \times 10^{-6}$. Most of this difference can be explained by the risetime transient of our square wave signal. The transient reduces the rms value of our signal relative to a perfect square wave. To estimate the correction we made an accurate oscillograph of the transient and numerically computed its rms value relative to a perfect square wave. The resulting correction is $(-22 \pm 5) \times 10^{-6}$. Thus, with the correction, we have $\delta = (-4 \pm 7) \times 10^{-6}$. This is consistent with the previously determined value of $\delta = (0 \pm 1) \times 10^{-6}$.

This comparison between a dc and a square wave input is very similar to the fast reversed dc measurements of Klonz, *et al.* [6], although our uncertainty is substantially greater, largely because of the low input voltage and the contribution of the transients to the rms value.

In our experiment the input voltages are derived directly from the Josephson effect and are therefore known with great accuracy. This feature is not critical to a dc-versus-square wave measurement but it will be important when the experiment is extended to the synthesis of a sine wave.

VI. CONCLUSION

The feasibility of programmable Josephson voltage standards for fast dc measurements and waveform synthesis has been demonstrated. A new SNS junction technology is being developed to make high critical current, self-shunted junctions, that have the noise immunity, $I_c R_N$ product, and output drive capability that are required to achieve practical waveform synthesis. Present devices are limited by the fabrication technology to a maximum output voltage of about 300 mV and are susceptible to transient induced magnetic flux trapping. We expect the flux trapping problem to be solved by improving the critical currents of wiring films and contacts within the circuit. As the fabrication yield improves, output voltages of 1V to 10 V should be possible. Sine waves synthesized from a programmable Josephson array will bypass the usual thermal methods and provide an ac standard that is derived directly from the international realization of the volt. In the near term, it is likely that programmable Josephson voltage standards will find their greatest use in fast automated dc measurements and in ac measurements at low voltages or frequencies where the performance of thermal voltage converters declines.

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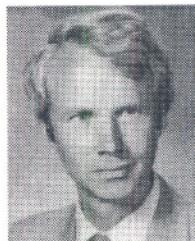
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Samuel P. Benz, photograph and biography not available at the time of publication.

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