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Nanotechnology for next generation Josephson voltage standards

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Abstract

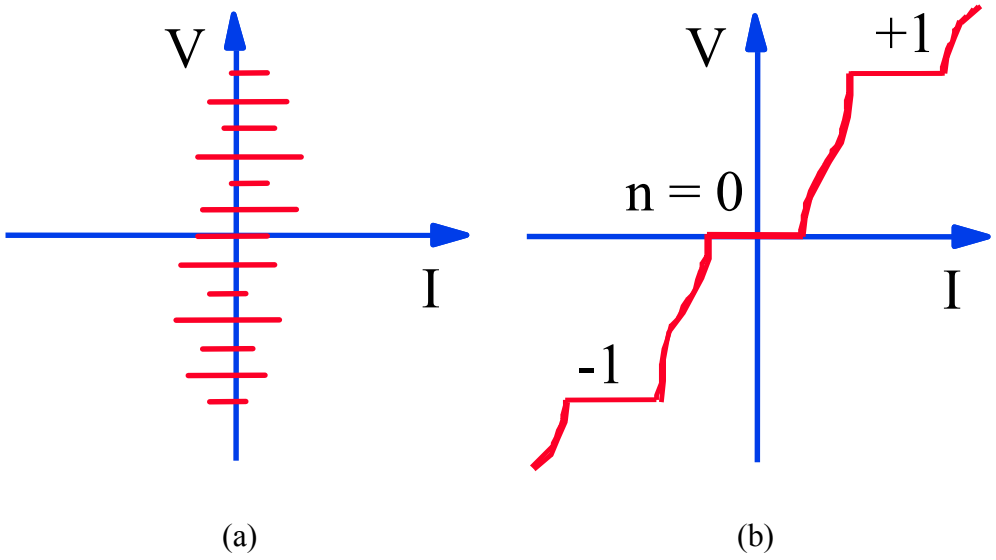
We have developed two voltage standard systems: the programmable Josephson voltage standard and the Josephson arbitrary waveform synthesizer. The programmable system is fully automated and provides stable programmable dc voltages from –1.2 V to +1.2 V. The synthesizer is the first quantum-based ac voltage standard source. It uses perfectly quantized Josephson pulses to generate arbitrary waveforms with low harmonic distortion and stable, calculable time-dependent voltages. Both systems are presently limited to output voltages less than 10 V as a result of frequency requirements and the limits of junction fabrication technology. We describe the development of fabrication technology for these systems and describe the circuit- and fabrication-related constraints that presently limit system performance. Finally, we propose the use of lumped arrays of junctions to achieve higher practical voltages through development of a nanoscale junction technology, in which 15,000 junctions are closely spaced at 50 nm to 100 nm internals.

I. Introduction

Josephson voltage standard systems have advanced over the past 30 years as a result of improvements in microelectronic fabrication as well as by clever physics and engineering ideas (see reviews by Kautz,[1] Niemeyer,[2] and Hamilton[3]). The basis for these systems is the superconducting Josephson junction.[4] When driven with a sinusoidal frequency f, a Josephson junction has a voltage-current characteristic with constant voltage regions given by $V_n = nhf/2e$, where n is an integer and $h/2e$ is the ratio of Planck's constant to twice the elementary charge. These values of V_n are directly

proportional to the frequency through fundamental constants only; these constant voltage step values are not dependent upon any environmental or material parameters. Since frequency can be accurately and stably controlled to parts in 10^{12}, a Josephson junction can convert frequency into accurate voltages.

The first Josephson voltage standards were single junctions. Since $h/2e \approx 2.07$ μV/GHz, single junction standards were only able to generate small voltages in the range from 1 mV to 10 mV for practical frequencies of 10 GHz to 100 GHz.[5] In order to achieve larger voltages, series arrays of junctions were attempted. In 1983 an array of 20 junctions succeeded in realizing a total voltage of 100 mV.[6] This feat was accomplished by independently current biasing each junction to ensure that each junction was on its respective constant voltage step. Independent biasing was necessary because junction fabrication technology at that time was unable to produce sufficiently identical junctions. Variations in junction dimensions (area) and barrier thickness result in variations in the voltage-current characteristics, thus requiring different junctions to have different bias conditions.



(a) (b)

Fig. 1. Voltage-current curves for different rf-driven Josephson junctions. (a) Zero-crossing steps of highly capacitive junction typical for conventional Josephson voltage standards. (b) Stable steps of a highly damped junction for programmable voltage standards.

In 1977 Levinson et al.[7] proposed a way to surmount the junction uniformity problems of the existing fabrication methods by using highly capacitive junctions. Such superconductor-insulator-superconductor (SIS) junctions have hysteretic voltage-current characteristics so that, when driven with a microwave frequency, their constant voltage steps intersect the zero-current axis. Since there are no stable regions between these zero-crossing steps, series arrays of highly capacitive junctions can be biased with a common current regardless of their non-uniform characteristics. This idea, among others, lead to the development of conventional Josephson voltage standards with large arrays of junctions.[8,9,10]

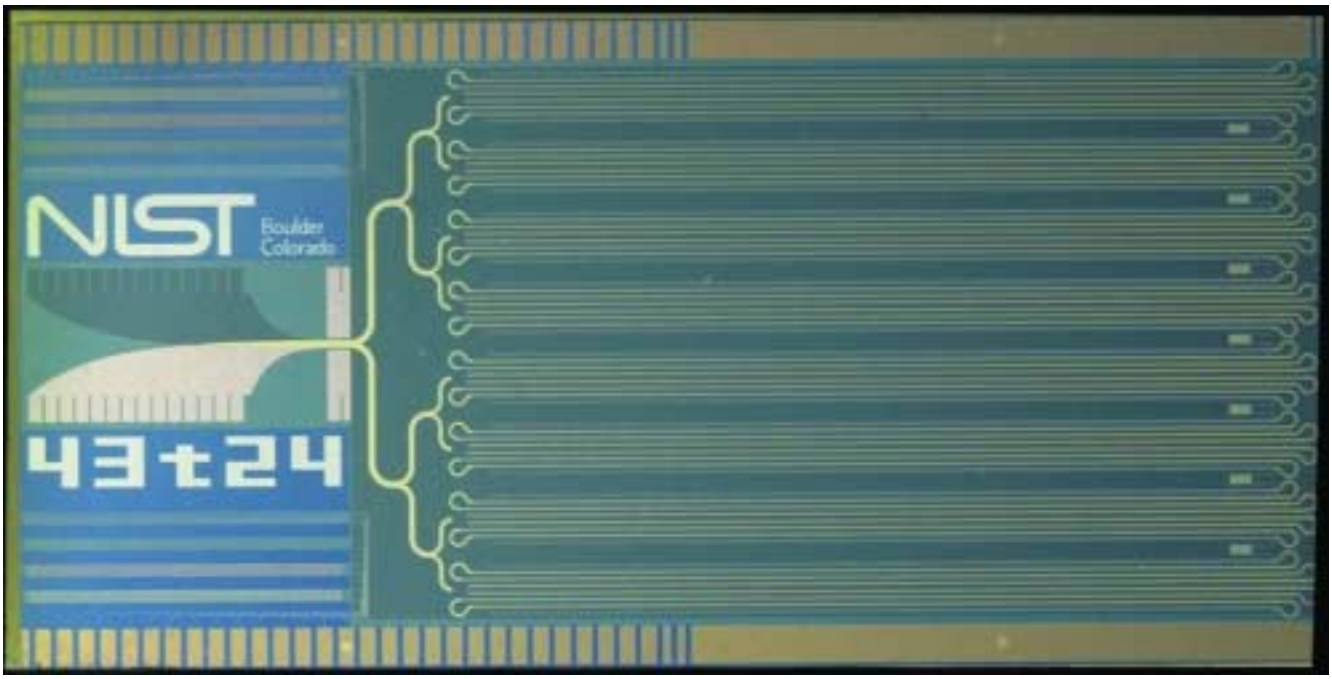


Fig. 2. Conventional 10 V Josephson voltage standard chip. Microwaves are launched onto the chip through the finline on the left side and then divided to drive 16 arrays of 1263 junctions each. The pads on the top and bottom are for a dc path that includes all 20 208 junctions in series.

Continued improvements in lithography and materials resulted in improved yield for these circuits with larger numbers of junctions.[11] For example, IBM's Josephson computer project led to improved junction oxide barriers and PbInAu superconducting electrodes.[12] Because the Pb-alloy junctions were subject to change with thermal cycling, efforts proceeded to develop an all-refractory junction process

using niobium for both junction electrodes and wiring. However, niobium oxide proved to be a poor junction barrier and yielded only moderate junction quality. The next major improvement occurred when Gurvitch, et al.[13] at Bell Labs discovered that thermally grown aluminum oxide barriers were extremely stable, resulting in the first Josephson high-quality junctions with excellent uniformity. Over the years, this all-refractory process with aluminum oxide barrier junctions has continued to improve with respect to junction uniformity and circuit yield. Using improved lithography and processing techniques, researchers world-wide continue to pursue the goal of large scale superconductive integrated circuits for high-performance superconductive digital electronics. All these advances have enabled the development of the present 10 V conventional Josephson voltage standard systems, which use chips having 20 000 or more junctions, where each Nb-Al_2O_3-Nb junction has an 18 μm × 30 μm area.[3]

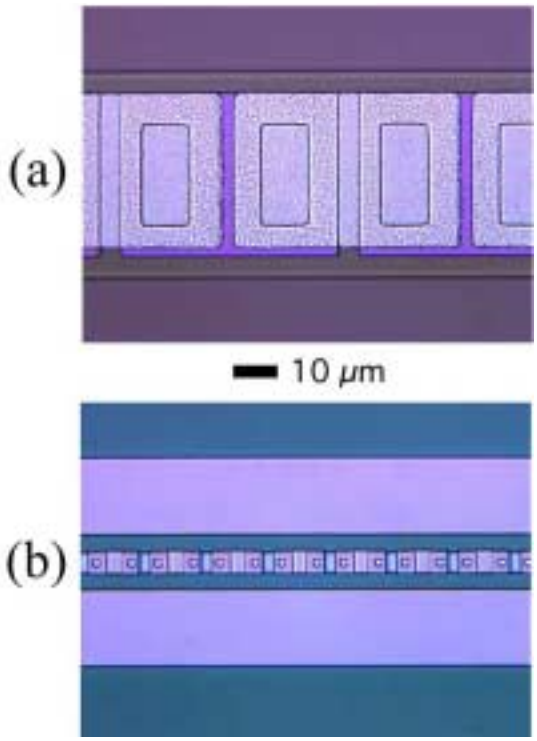


Fig. 3. Comparison of (a) 20 year-old conventional Nb-Al_2O_3-PbInAu 18 μm × 30 μm SIS junctions with (b) Nb-PdAu-Nb 2 μm × 2 μm SNS junctions. Minimum feature sizes are via holes in the insulating layer that allow superconducting wiring to connect adjacent junctions: (a) 10 μm × 24 μm

and (b) 1 μm × 1 μm. The SNS junctions (b) are distributed in series along the 6 μm-wide center conductor of a coplanar waveguide.

II. Programmable Voltage Standard

In 1995, Hamilton et al. suggested a quantum-based ac voltage standard using a Josephson digital-to-analog converter.[14] By dividing a large array into a binary sequence of independently biased smaller arrays, it was hoped that the circuit would be capable of rapidly selecting stable arbitrary dc voltages as well as ac waveforms with a calculable rms voltage. This required the development of highly damped Josephson junctions with non-hysteretic voltage-current characteristics. Such junctions have constant voltage steps that are single valued, so that individual constant voltage steps can be chosen using predetermined bias currents. This idea for a new voltage standard renewed our interest in developing uniform intrinsically shunted junctions for array applications, specifically in superconductor-normal metal-superconductor (SNS) junctions. Expectations were not high with regard to junction uniformity since critical current density is exponentially dependent upon the barrier thickness and sputter-deposited metal films are not as uniform as thermally grown oxides. Nevertheless, moderately thick 30 nm to 40 nm barriers of PdAu provided sufficient uniformity with appropriate junction characteristics.[15,16] However, the high current densities (2 mA/μm^2 to 4 mA/μm^2) require small junction areas (1 μm^2 to 4 μm^2) to maintain junction critical currents less than 10 mA. Fortunately, the large critical currents yield correspondingly larger current ranges for the constant voltage steps. This improves the operating margins for the circuits and allows for dramatically improved noise immunity compared to that of hysteretic junctions in conventional voltage standards, which have critical currents of only ~100 μA. The present 1 V programmable voltage standard system uses a chip shown in Fig. 4 with 32 768 Nb-PdAu-Nb junctions.[17] The 2 μm × 2 μm junctions have critical currents of ~8 mA and resistances of ~3 mΩ. The smallest features in the circuit are 1 μm diameter vias for wiring contacts to each junction.

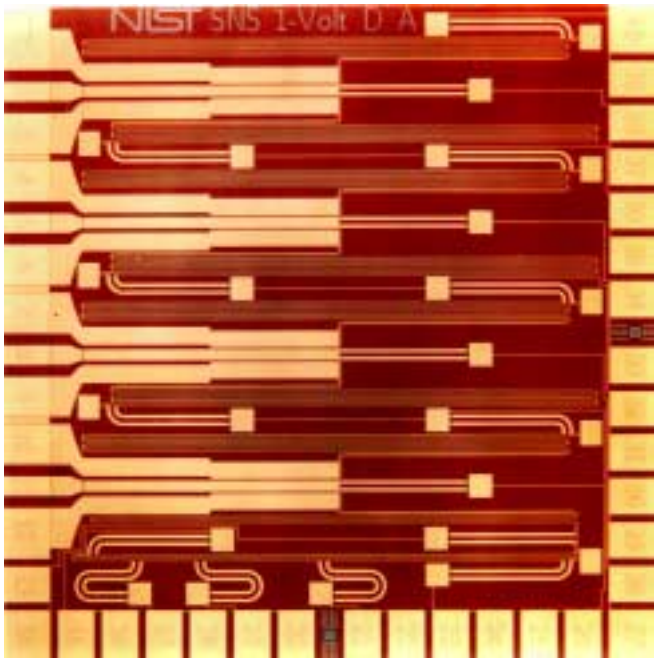


Fig. 4. 1 cm × cm NIST 1 V programmable voltage standard chip. Microwave are launched onto the chip on the four coplanar waveguide lines on the left side. The pads along the bottom and right sides are for dc bias lines to each array. There are 8 arrays of 4096 junctions each. The bottom array is divided into a binary sequence of 2048, 1024, 512, 256 and two arrays of 128 junctions.

One of the remaining challenges is to create a programmable standard capable of generating large voltages, like the 10 V of the conventional standard. Generating large voltages requires maximizing both the microwave frequency and the number of junctions. Operating margins, on the other hand, depend on both the junction uniformity and the uniformity of the microwave power applied to all junctions. Series arrays of junctions are typically distributed along a microstrip transmission line or a coplanar waveguide. Such distributed arrays are used for many of our designs. For example, the 1 V programmable chip uses arrays of 4096 junctions in each of eight parallel 50 Ω coplanar waveguides.[17]

There are many parameters that must be adjusted in order to optimize a distributed array for output voltage and operating margins. Kautz showed that the maximum junction diameter for planar SNS junctions is about 4 times the Josephson penetration length. For larger diameters, current nonuniformity through the junction dramatically affects the junction characteristics.[18] For Nb-PdAu-Nb junctions this limits the maximum critical current I_c to about 10 mA. It has also been shown that the

sinusoidal drive frequency that gives the largest operating margins for an array of nonuniform junctions should be between one and two times the junction characteristic frequency, $f = (1\text{-}2)\, f_c$, where the characteristic frequency is $f_c = 2eI_cR/h$ and R is the junction resistance.[19, 20] Because the junctions are dissipative, the number of junctions that can be placed in a transmission line of a certain impedance is limited by the microwave attenuation that can be tolerated for an acceptable reduction in operating margins. For an array of N junctions with resistance R per junction, the total rf-voltage drop across the array due to junction dissipation is approximately $1\text{-}\exp(-NR/2Z)$, where $Z = 50\ \Omega$ is the transmission line impedance.[21, 22] The transmission line must also be properly terminated to prevent standing wave reflections that would further degrade the microwave uniformity.

We can achieve optimum performance for a distributed array using the following procedure. Choose the $2eI_cR/h$ product to match the desired maximum drive frequency. This determines the required junction barrier thickness. Next, select the junction area to achieve the maximum critical current of 10 mA. Maximizing the critical current in turn minimizes the junction resistance and decreases the dissipation. As an example, the voltage drop due to dissipation is only 12% across a 4096-junction array of 3 mΩ junctions. 88% of the power is dissipated in the termination resistor. If we demand the same operating margins by always (1) choosing the same ratio $\alpha = NR/2Z$, (2) matching the I_cR product to the frequency, and (3) maximizing the junction critical current to 10 mA, then the number of junctions that can be placed in the transmission line decreases with increasing frequency, $N = 4e\alpha ZI_c/hf$. Thus, increasing the drive frequency cannot independently achieve larger output voltages for distributed arrays, although it may improve circuit yield by reducing the number of junctions.

Since dissipation limits the number of junctions in a transmission line, multiple arrays are generally used to increase the total output voltage. Through the use of fixed-frequency microwave elements, such as quarter wave taps and impedance transformers, the microwave power can be applied in parallel to

smaller arrays in these circuits while these smaller arrays can all be connected in series to create one large array with a high total output voltage. It is critical that the dc bias taps that connect the arrays behave as a high impedance at the sine wave frequency and as a superconducting short for dc; otherwise standing waves develop in the transmission line, reducing microwave power uniformity and operating margins for the arrays. This technique is used in both conventional voltage standards at 75 GHz[8] and in the programmable voltage standards at 16 GHz.[15]

Fig. 5. Programmable voltage standard system. The low-thermal probe is in the Dewar at left. The electronics in the middle (from top to bottom) include a digital voltmeter, dc bias electronics, computer, and microwave source. The system is fully automated.

Another method to achieve large stable voltages was discovered by researchers at PTB, who succeeded in demonstrating stable 10 V steps using SINIS junctions[23] with non-hysteretic voltage-current characteristics.[24,25] The 100 mΩ SINIS junctions are in a low-impedance 5 Ω transmission line, so there is significant dissipation. However, junctions on the microwave-driven end of the transmission line actively contribute to lock additional junctions farther down the transmission line.

Although the binary-sequence design for programmable voltage standards has proven adequate for *fast* and stable *dc* voltages, it is not practical for generating *ac* waveforms.[26] Since the switching time

of each bias current driver is limited to about 1 μs, there is a significant uncertainty in the average voltage during this time interval. Thus the binary programmable voltage standard system is primarily used for applications that require stable and programmable dc voltages such as watt-balance experiments[27,28] and fast-reversed dc to dc comparisons.[29,30]

III. Josephson Arbitrary Waveform Synthesizer

In order to create a quantum-based ac Josephson voltage standard, the Josephson arbitrary waveform synthesizer was developed to again exploit the perfect quantization of Josephson junctions.[31,32,33] However, instead of being concerned with the constant voltage steps of a sinusoidally driven junction, we consider the Josephson junction as a device that generates perfectly quantized voltage pulses. The time-integrated area of every Josephson pulse is precisely equal to $h/2e$. Digital synthesis techniques and precise control of the timing of every pulse allows the generation of voltage waveforms with unprecedented accuracy and stability. Simulations and experiments have shown that voltage noise and timing jitter, intrinsic to all semiconductor-switched digital code generators, create harmonic distortion in a synthesized waveform. We have shown that the perfect area quantization of Josephson pulses can recover the low harmonic distortion of the original digital code that was created assuming perfect voltage levels and perfect timing.[33] Using this system, we have demonstrated a technique for increasing the output voltage of pulse-driven arrays and for synthesizing bipolar waveforms by combining a high-speed digital signal with a sine wave.[34,35] We have also demonstrated synthesized arbitrary waveforms[36] with arrays of 4096 junctions up to peak voltages of 60 mV and we have reduced undesirable distortion-induced harmonics to 95 dB below the fundamental. Finally, we have performed preliminary rms ac-dc and ac-ac voltage comparisons on 250-junction arrays at a much smaller voltage of 3.7 mV.[37]

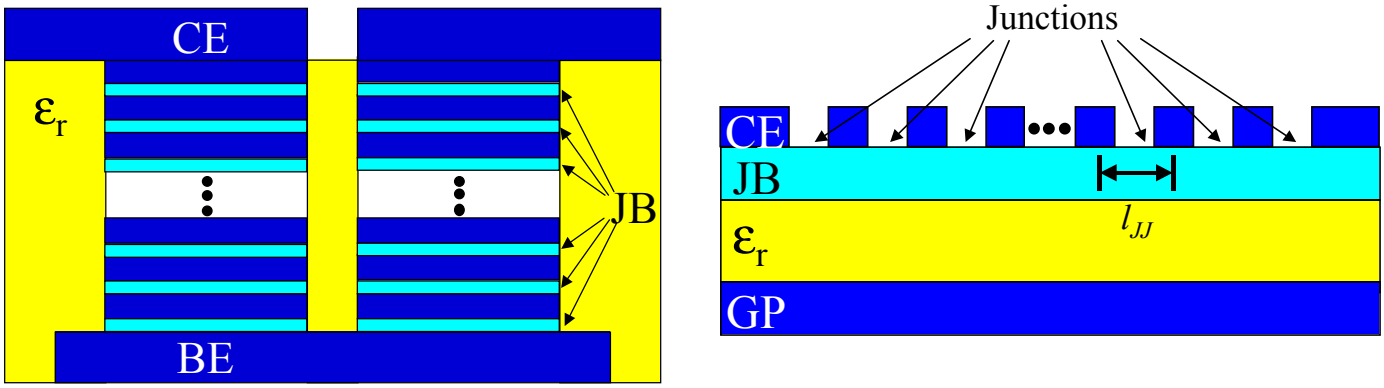
However, achieving practical voltages of 1 V to 10 V is even more difficult than for the programmable voltage standard. The fixed-frequency elements that are used in the sine wave-driven

circuits cannot be used in the Josephson arbitrary waveform synthesizer because the digital code is inherently broadband. For this circuit, all harmonic components of the digital code from dc to 18 GHz must remain in the microwave transmission line circuit driving the array. We have addressed this problem by developing 60 MHz low pass filters for the low-frequency taps.[36,37] It is important that these filters have few resonances and sufficient power handling at microwave frequencies. Unfortunately it will be difficult to drive many arrays in parallel and connect them in series for low frequencies due to the difficulty in providing many parallel broadband signals with sufficient output power. It is not cost effective to have multiple code generators. Furthermore, power splitters and amplifiers are generally not sufficiently broadband for this application.

IV. Lumped Arrays

In order to increase the output voltage for both programmable and ac voltage standards (which are limited by dissipation, broadband behavior, and in general, the physics of distributed arrays), we have begun developing nanoscale junctions for lumped arrays.[38] A lumped array is one in which all of the junctions are placed in the transmission line within a small fraction, say one-eighth to one-quarter, of the wavelength of the highest frequency of interest. Our goal is to make an array whose total impedance is equal to the 50 Ω transmission-line impedance. The output voltage would then be increased by about a factor of 8. These arrays would also be very efficient since most of the broadband power would not be wasted in a termination resistor as in distributed array circuits. Using the same arguments we used previously to optimize distributed arrays, if the maximum drive frequency is twice the characteristic junction frequency, then the maximum output voltage is $V_{max} = 2ZI_c$. For a 50 Ω transmission line and 10 mA critical current, this yields a 1 V maximum output voltage for a single array. This approach could increase the output voltage of the Josephson arbitrary waveform synthesizer to 1 V and also the programmable voltage standard output voltage to 10 V.

The challenge for lumped arrays is that the junctions must be very close together. The effective dielectric constant for a coplanar waveguide on Si is 6.4. An 18 GHz drive frequency then has a quarter wavelength of 1.6 mm. A critical current-resistance product of 37 μV and a critical current of 10 mA implies a junction resistance of 3.7 mΩ. Thus, a 50 Ω array would then require 13 500 series junctions spaced about 120 nm apart on the coplanar wavequide. This is a significant challenge, since the smallest SNS arrays fabricated using our present process have junction spacings of 7 μm. These lumped array junctions will require nanoscale dimensions and control to achieve sufficient uniformity.



a) Stacked junctions b) In-line junctions.

Fig. 6. Lumped array fabrication concepts. (a) Stacked SNS junctions. (b) In-line SNS junctions. Counter electrode (CE), base electrode (BE), ground plane (GP), and other Nb superconductor between barriers are in blue. The junction barriers (JB) are in light blue. The insulating dielectric (ε_r) is yellow.

We are developing two different junction geometries for these lumped arrays: stacked junctions and in-line junctions. For the stacked junctions shown in Fig. 6(a), multiple barriers are deposited alternately with superconducting layers to create stacks of two-dimensional junctions. The lumped array in this geometry would have 270 stacks of 50 junctions each. The stacks would be 2 μm to 4 μm on each side and spaced 6 μm apart. It will be a challenge to ensure that these 6 μm tall stacks have vertical sidewalls and to achieve a thick planarized insulator for the wiring contacts. The in-line junction geometry shown in Fig. 6(b), on the other hand, begins with a ground plane and an insulator, followed by a normal metal-superconductor bilayer. The 20 nm to 40 nm long by 1 μm to 10 μm wide

trenches in the top superconductor can be etched by a number of techniques, including focused ion beam[39] or reactive ion etching of a previously e-beam defined pattern. Proximity coupling between the superconducting islands occurs through the lower normal metal layer. The ground plane ensures uniform current flow through these relatively wide junctions. Heat dissipation from these lumped arrays may be a problem and the close spacing of these junctions may be influenced by quasiparticle coupling or other effects.

V. Conclusion

We have reviewed some of the major events in the development of fabrication technology for Josephson voltage standards. We describe the issues related to operating performance for the programmable voltage standard and the Josephson arbitrary waveform synthesizer. Finally, we propose the use of lumped arrays of Josephson junctions as a way to increase the output voltage and improve the performance of voltage standard systems.

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