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A SYSTEM TO MEASURE CURRENT TRANSDUCER PERFORMANCE

Bryan C. Waltrip, Thomas L. Nelson
National Institute of Standards and Technology[1]
Gaithersburg, MD 20899

Abstract

A special purpose ac current transducer measurement system capable of intercomparing transducers with ac output voltage ratios from 1:1 to 50:1 has been developed to extend the range and accuracy of current transformer, current shunt, and mutual inductor calibrations at power frequencies of 50 Hz and 60 Hz. The system consists of a two-stage binary inductive voltage divider, an amplifier-aided two-stage current transformer, a precision shunt, a wideband buffer, and a commercial, sampling digital multimeter (DMM). When comparing current transducers with ac output voltage ratios of 1:1 to 50:1, the system attains an overall relative standard uncertainty of the ratio of 10^{-5} to 10^{-4}, respectively. The basic system can be used to calibrate transducers with input currents of 0.1 A to 200 A (RMS) and can be extended to measure devices handling input currents up to 15 kA.

Summary

Introduction

A limiting factor concerning the accurate determination of the ratio and phase errors of various types of current transducers, or ac current-to-voltage converters, is that of comparing the converter under test to a standard converter in conditions where the transadmittance of the two devices differ by a significant degree. Common approaches to cover the wide dynamic range in currents are to design bridges that include current transformers and current comparators with many taps, or include a large number of standard resistive shunts. While bridges of this type can be quite accurate over a wide range of currents and frequencies [1], they are generally difficult and expensive to design, operate, and maintain.

The advent of sophisticated, high-accuracy, commercial waveform sampling systems has made it practical to significantly reduce the complexity of a shunt comparison bridge. A less complex bridge has been designed by transferring the in-phase and quadrature error component determinating hardware from the usual current-comparator/detector arrangement to a commercial DMM.

Operating Principle

The basic bridge for operation with primary input currents from 0.1 A to 200 A is shown in Fig. 1.

A commercial digital signal generator, along with transconductance amplifier, A_1 [2], are used to generate the test current, I, which is applied to both the device under test (DUT) and an amplifier-aided, two-stage current transformer, T_1 [3]. Depending upon measurement requirements, the test current, I, is scaled by the current transformer, T_1, resulting in a reference current, I_R, through a wideband 4-terminal current shunt, Z_R [1]. The reference voltage, $V_R = I_R Z_R$, is then compared to the output voltage, V_U, of the DUT using a commercial sampling DMM and switch SW_1, where the sampled signal data is then downloaded via an IEEE-488 bus to the system controller, PC.

The system controller software utilizes a least-squares waveform amplitude and phase estimation algorithm, as discussed in [4]. The hardware has been designed to optimize the least-squares algorithm over a wide dynamic range of V_U/V_R. A wideband high-impedance two-stage buffer amplifier, A_3, is used to buffer the test signals from the input of a binary inductive voltage divider (BIVD), T_2 [6]. This amplifier features extremely low amplitude and phase errors in the 50 Hz to 60 Hz frequency range [5]. The BIVD is adjusted to equalize the amplitudes of the V_R and V_U signals sampled by the DMM. This equalization has the effect of minimizing any amplitude-dependent phase errors present in the DMM's input circuitry. The very high input impedance (>10 MΩ) of the DMM when in its dc voltage measurement mode helps to minimize loading effects on the BIVD by the DMM. In addition, phase information between the sampled V_R and V_U signal records is maintained by triggering the DMM with the signal generator's external synchronization signal.

Test Results

Verification at 50 Hz and 60 Hz of the SW_1, A_3, T_2, and DMM hardware configuration shown in Fig. 1 was accomplished by substituting the V_U and V_R signals with the input and output voltages of an inductive voltage divider (IVD). The IVD was then adjusted to ratios between 1:1 and 1:50. The sampling system's estimation

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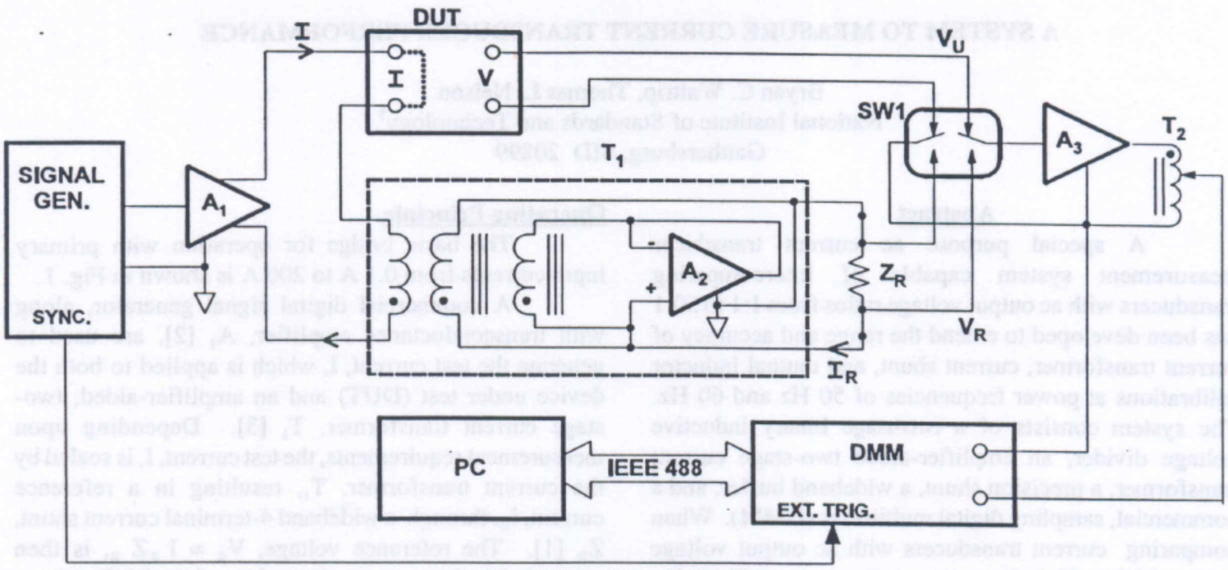


Fig. 1. Detailed circuit diagram.

of the ratio and phase showed agreement with the IVD setting to within the relative standard uncertainty of the IVD and the relative standard uncertainty of the sampling system's measurements due to random effects, which were 10^{-5} for 1:1 signal ratios and 10^{-4} for 1:50 signal ratios. In addition, the complete measurement system was compared to a current comparator-based system. Again, agreement between the two systems was within the relative standard uncertainty of the current comparator-based system and the relative standard uncertainty of the sampling system's measurements due to random effects.

A more complete analysis of system design and performance will be presented in the final paper.

References

[1] T. M. Souders, "An Audio-Frequency Four-Terminal Resistance Bridge," *IEEE Trans. Instrum. Meas.*, vol. IM-23, no. 4, pp. 342-345, Dec. 1974.

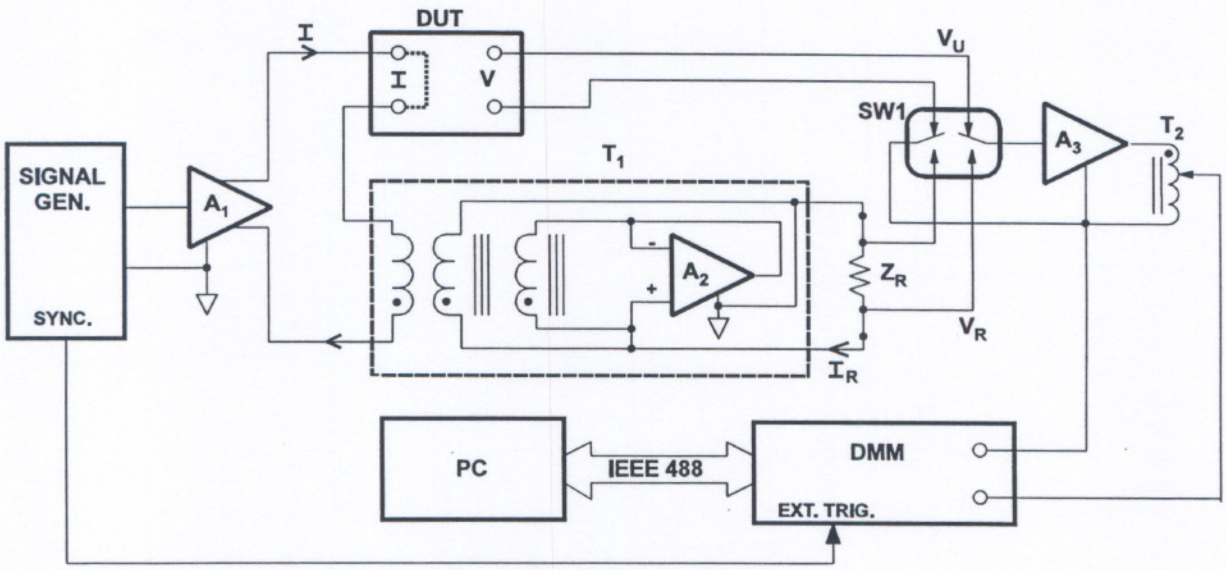
[2] O. Laug, "A 100 A, 100 kHz Transconductance Amplifier," *IEEE Trans. Instrum. Meas.*, vol. 45, no. 3, pp. 440-444, June 1996.

[3] T. M. Souders, "Wide-Band Two-Stage Current Transformers of High Accuracy," *IEEE Trans. Instrum. Meas.*, vol. IM-21, no. 4, pp. 340-345, Nov. 1972.

[4] B. Waltrip, M. Parker, N. Oldham, and B. Bell, "The NIST Sampling System for the Calibration of Phase Angle Generators from 1 Hz to 100 kHz," *Conference Proceedings, 1992 NCSL Workshop and Symposium*, pp. 613-616, Aug. 1992.

[5] B. Waltrip, N. Oldham, "Wideband Wattmeter Based on RMS Voltage Measurements," *IEEE Trans. Instrum. Meas.*, vol. 46, no. 4, pp. 781-783, Aug. 1997.

[6] S. Avramov, N. Oldham, D. Jarret, B. Waltrip, "Automatic Inductive Voltage Divider Bridge for Operation from 10 Hz to 100 kHz," *IEEE Trans. Instrum. Meas.*, vol. 42, no. 2, pp. 131-135, April 1993.



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