SIMULATING THE DYNAMIC ELECTRO-THERMAL BEHAVIOR OF POWER ELECTRONIC CIRCUITS AND SYSTEMS [†]

by

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Abstract – A methodology is presented for simulating the dynamic electro-thermal behavior of power electronic circuits and systems. In the approach described, the simulator simultaneously solves for the temperature distribution within the semiconductor devices, packages, and heatsinks (thermal network) along with the currents and voltages within the electrical network. The thermal network is coupled to the electrical network through the electro-thermal models for the semiconductor devices. The electro-thermal semiconductor device models calculate the electrical characteristics based upon the instantaneous value of the device silicon chip surface temperature and calculate the instantaneous power dissipated as heat within the device. The thermal network describes the flow of heat from the chip surface through the package and heatsink and thus determines the evolution of the chip surface temperature used by the semiconductor device models. The thermal component models for the device silicon chip, packages, and heatsinks are developed by discretizing the nonlinear heat diffusion equation and are represented in component form so that the thermal component models for various packages and heatsinks can be readily connected to one another to form the thermal network.

I. Introduction

Effective simulation of power electronic circuits requires the availability of accurate models for the power semiconductor devices in the simulators used by circuit and system designers. Because the structures of power devices are significantly different than their micro-electronic integrated circuit counterparts, the semiconductor models in most commercial circuit simulators do not adequately describe the behavior of power devices. Recently though, accurate physics-based power semiconductor models have been implemented into circuit and system simulation programs [1-5] and characterized power device part numbers have been included in simulator component libraries [2,4]. However, the device temperature is a critical parameter in determining the electrical behavior of power devices because the devices dissipate a considerable amount of heat and are often operated in high temperature environments. In addition, the simulation of electro-thermal behavior is important in the design of power modules and power circuit boards due to the thermal coupling between adjacent semiconductor devices.

Although the traditional micro-electronic semiconductor device models include temperature dependence, the temperature used by the device models in programs such as SPICE (Simulation Program with Integrated Circuit Emphasis) must be chosen by the user prior to the simulation and hence must remain constant at the predetermined value during the simulation. The unique approach taken in this work is to define the temperatures at various positions within the silicon chips, packages, and heatsinks (thermal network) as simulator system variables so that the dynamic temperature distribution within the thermal network is solved for by the simulator in the same way as the node voltages within the electrical network are solved. Because the device electrical characteristics depend upon the instantaneous temperature calculated from the thermal network models, the dynamic self-heating is accounted for and the dynamic heating of adjacent devices can be described (e.g., thermal coupling between devices in a power module or on a common heatsink).

The purpose of this paper is to describe the new methodology for simulating the dynamic electro-thermal behavior of power electronic circuits and systems. The new methodology enables the designer to incorporate thermal management considerations into the design of electronic systems. For example, the designer can readily interchange semiconductor devices having similar electrical characteristics but with different chip areas and thus different thermal characteristics. The designer can also interchange thermal network components such as packages and heatsinks and can change the topology of the thermal components within the thermal network. For example, the behavior of a system including thermal coupling between adjacent electrical devices mounted on a single heatsink can be compared with the behavior of the same system but with the devices having separate heatsinks. In this paper, the methods used to develop the electro-thermal semiconductor device models and the thermal network component models are given, and the methods used to implement these models into the Saber[‡] circuit simulator are described. Examples are also given to demonstrate the accuracy, computational efficiency, and ease of use of the new methodology.

II. Electro–Thermal Simulation Methodology

Figure 1 is a diagram of the electro-thermal network simulation methodology indicating that the electrical and thermal networks are coupled through the electro-thermal models for the semiconductor devices. The electro-thermal models for the semiconductor devices (IGBTs and power diodes in Fig. 1) have electrical terminals that are connected to the electrical network and a thermal terminal that is connected to the thermal network. The thermal nodes in the thermal network have units of temperature (K) across the nodes and units of power (W) flowing through the nodes, whereas the through and across variables for electrical networks are current and voltage. The thermal network is represented using thermal network component models so that the thermal models for different packages and heatsinks can be readily interconnected in the same way that the electrical network components are interconnected. The thermal network models for power modules and heatsinks contain multiple termi-

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nals and account for the thermal coupling between the adjacent semiconductor devices.

As an example, Fig. 2a is a schematic of an electro-thermal network, and Fig. 2b is the corresponding Saber simulator netlist using the IGBT electro-thermal model [6] and the thermal component models of the silicon chip, the T0247 package, and the TTC1406 heatsink [7]. The first column of the Saber netlist in Fig. 2b specifies the name of the template that contains the model equations for each component (left-hand side of the period) and the instance within the circuit (right-hand side of the period). The remaining columns on the left-hand side of the equal sign indicate the terminal connection points of the components within the network, where the electro-thermal IGBT model is connected to both the electrical and thermal networks. The parameters used by the model templates to describe the specific components are listed on the right-hand side of the equal sign. For example, the temperature coefficients of the IGBT base lifetime and transconductance parameter are changed from the default values. It is evident from Fig. 2 that the thermal network component models developed in this work are interconnected to form the thermal network in the same way as the electrical components are interconnected to form the electrical network.

An advantage of the new methodology is that the interconnection of the thermal and electrical components are easily changed so that the system designer can readily examine different electrical and thermal network topologies and can easily exchange different thermal and electrical component types. To simplify the system design process, the thermal component models are represented in the same form as the electrical component models, and the details of the thermal component model physics are transparent to the user. However, the structural and physical parameters of the thermal models enable the user to provide the specific information necessary to perform accurate simulations. Furthermore, by connecting the thermal terminal of the electro-thermal semiconductor device models to a constant temperature source, the models reduce to the traditional global temperature-dependent models used for traditional electrical network simulation. Thus, the traditional semiconductor models can be completely replaced by the electro-thermal semiconductor models so that design engineers can incorporate the thermal management considerations at any point in the traditional electrical network design process.

Because the time constants for heat flow within the silicon chip, package, and heatsink are many orders of magnitude longer than the time constants of the electronic devices and circuits, the self-heating effects behave dynamically even for circuit conditions that are considered to be static for the electronic devices. In addition, for circuit conditions that result in high power dissipation levels, the heat is applied rapidly to the chip and only diffuses a few micrometers into the chip surface. Therefore, the chip-heating process is non-quasi-static, and the temperature distribution within thermal network depends upon the rate at which the heat is applied. The thermal network component models used in this work accurately describe the dynamic temperature distribution in the thermal network for the full range of applicable power dissipation levels. The new dynamic electro-thermal network simulation methodology provides a procedure for developing accurate and computationally efficient thermal network component models and electro-thermal semiconductor models. The simulation speed for typical electro-thermal network simulations is comparable to that of the electrical network alone for the same simulation interval.

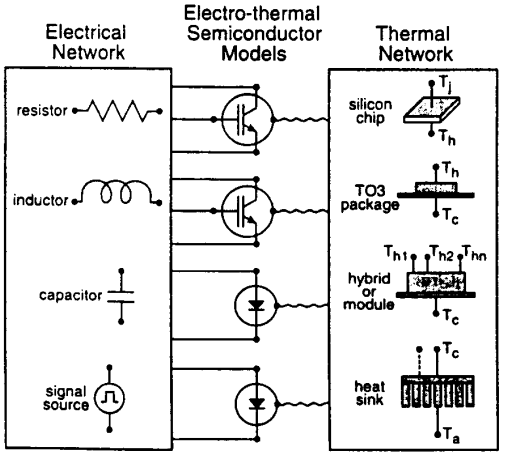
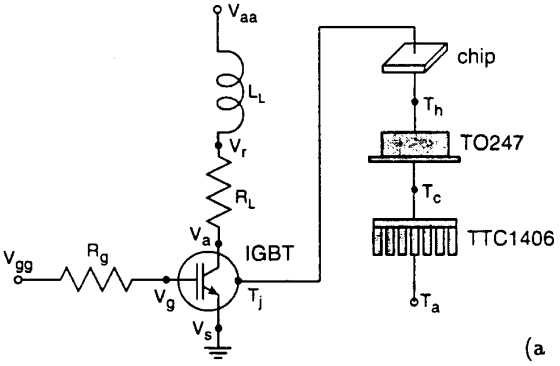


Fig. 1. Diagram indicating interconnection of electrical and thermal networks through electro-thermal models for semiconductor devices.




```
#IGBT electro-thermal simulation

#Electronic network components
v.vaa          vaa  0          = 300
l.ll           vaa  vr         = 80u
r.rl           vr   va         = 30
r.rg           vgg  vgs        = 10
pulsgen.1      vgg  0          = 20

#IGBT electro-thermal model
igbt_therm.1   va   vgs  0  tj = tauhl_1=1.6,
                                 kp_1=1.5

#Thermal network components
chip_therm.1       tj   th     = thick=0.05,
                                 a_chip=0.1
to247_therm.1      th   tc     = a_chip=0.1
ttc1406_therm.1    tc   ta     = a_heat=0.4
t.ta               ta   0      = 300
```

(b

Fig. 2. a) Schematic and b) Saber netlist of an example electro-thermal network.

III. Electro–Thermal Semiconductor Models

The electro-thermal semiconductor device models couple the electrical and thermal networks. Figure 3 is a diagram of the structure of the electro-thermal semiconductor device models indicating the interaction with the thermal and electrical networks through the electrical and thermal terminals, respectively. The electro-thermal semiconductor models use the instantaneous device temperature (temperature at the silicon chip surface T_j) to evaluate the temperature-dependent properties of silicon and the temperature-dependent model parameters. These temperature-dependent values are then used by the physics-based semiconductor device model to describe the instantaneous electrical characteristics and the instantaneous dissipated power. The network simulator solves the system of electro-thermal equations by iterating the system variables (electrical node voltages, thermal node temperatures, and explicitly defined system variables) until the components of currents into each electrical node sum to zero (Kirchhoff's current law) and the components of power flow into each thermal node sum to zero (energy conservation). In the remainder of this section, the Saber electro-thermal IGBT model is used as an example [6].

The temperature-dependent expressions for the physical properties of silicon are given in Table 1 and the temperature-dependent IGBT model parameters are given in Table 2 [6]. The empirical expressions of Table 2 are developed using the extracted values of the model parameters versus temperature [8]. An accurate extraction sequence [1,2] is required to resolve the temperature dependence of the IGBT model parameters. The parameters in Table 2 with subscript 0 are the extracted values of the model parameters at the nominal temperature T_0, and the parameters with subscript 1 are the extracted temperature coefficients of the IGBT model parameters. The advantage of using a physics-based model for the power semiconductor devices is that the well-known temperature-dependent properties of silicon can be used to describe the temperature dependence of the model, and only a few temperature-dependent model parameter expressions must be developed. However, for models that rely heavily on empirical-based formulas, each of the empirical formulas must be calibrated versus temperature. Therefore, it is recommended that the electro-thermal models be developed using models that are derived directly from semiconductor device physics without unsubstantiated approximations.

To implement electro-thermal models into the Saber circuit simulator, the components of current into electrical nodes and the components of power into thermal nodes are expressed in terms of simulator system variables. System variables for electro-thermal models are the electrical node voltages, thermal node temperatures, and other system variables defined to solve implicit model equations. Figure 4a is the equations section of the Saber electro-thermal IGBT model, and Fig. 4b is an analog circuit representation of the Saber electro-thermal IGBT model equations where the components of power dissipation are indicated by dashed lines. The first six statements in Fig. 4a specify the components of current between the device electrical terminals and the internal electrical nodes, and the next five statements specify implicit model functions [3]. Finally, the last statement in Fig. 4 specifies the power delivered to the thermal terminal (tnode). The model functions used in the equations section, e.g., Qgs, Cgd, Imos,..., and power of Fig. 4 are evaluated in terms of the system variables in the values section of the Saber IGBT electro-thermal template.

To incorporate the electro-thermal effects into the Saber IGBT model described in ref. [3], the expressions in Tables

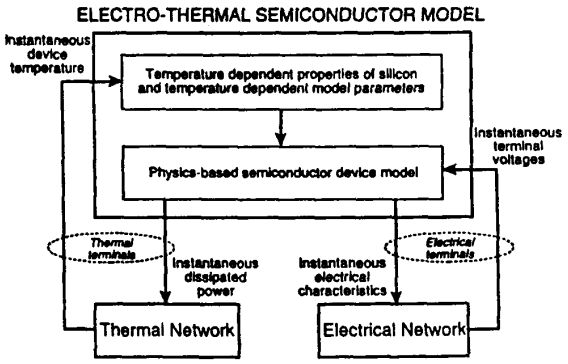


Fig. 3. Diagram of the structure of the electro-thermal semiconductor device models.

TABLE 1
Temperature–Dependent Properties of Silicon

$$\mu_n(T_j) = 1500 \cdot (300/T_j)^{2.5} \quad (T1.1)$$

$$\mu_p(T_j) = 450 \cdot (300/T_j)^{2.5} \quad (T1.2)$$

$$D_n(T_j) = \mu_n \cdot kT_j/q \quad (T1.3)$$

$$D_p(T_j) = \mu_p \cdot kT_j/q \quad (T1.4)$$

$$n_i(T_j) = 3.88 \times 10^{16} \cdot (T_j)^{1.5} / \exp(7000/T_j) \quad (T1.5)$$

$$v_{nsat}(T_j) = 10^7 \cdot (300/T_j)^{0.87} \quad (T1.6)$$

$$v_{psat}(T_j) = 8.37 \times 10^6 \cdot (300/T_j)^{0.52} \quad (T1.7)$$

$$\alpha_1(T_j) = 1.04 \times 10^{21} \cdot (T_j/300)^{1.5} \quad (T1.8)$$

$$\alpha_2(T_j) = 7.45 \times 10^{13} \cdot (T_j/300)^2 \quad (T1.9)$$

$$BV_k(T_j) = 5.34 \times 10^{13} \cdot (T_j/300)^{0.35} \quad (T1.10)$$

TABLE 2
Temperature–Dependent IGBT Parameters

$$\tau_{HL}(T_j) = \tau_{HL0} \cdot (T_j/T_0)^{\tau_{HL1}} \quad (T2.1)$$

$$I_{snc}(T_j) = \frac{I_{snc0} \cdot (T_j/T_0)^{I_{snc1}}}{\exp[14000 \cdot (1/T_j - 1/T_0)]} \quad (T2.2)$$

$$V_T(T_j) = V_{T0} + V_{T1} \cdot (T_j - T_0) \quad (T2.3)$$

$$K_p(T_j) = K_{p0} \cdot (T_0/T_j)^{K_{p1}} \quad (T2.4)$$

1 and 2 are added to the beginning of the values section of the Saber IGBT template, and the temperature coefficients are added to the template parameter list. The model functions used to calculate the electrical characteristics (Table 1 of ref. [3]) are then evaluated using these temperature-dependent quantities, whereas in the traditional approach used in the nonelectro-thermal Saber IGBT model, these quantities are model parameters that do not change value during simulation. Finally, the expression for the dissipated power is calculated at the end of the values section of the Saber electro-thermal IGBT template using the temperature-dependent model functions. The dissipated power must be calculated using the internal components of current as indicated in Fig. 4b and not simply the terminal currents and voltages, because the power delivered to internal device capacitances is not dissipated immediately as heat but is stored in the electric field energy of the capacitors [6].

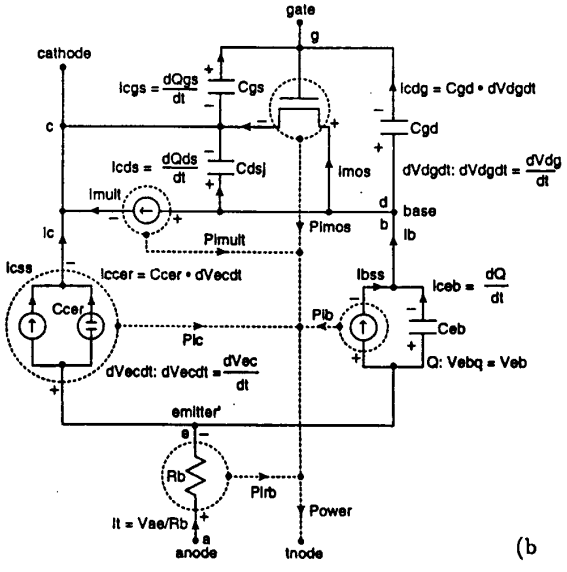
```
equations {
    i(gate - > cathode)    +=                          d_by_dt(Qgs)
    i(drain - > gate)      +=                    Cgd * dVdgdt
    i(drain - > cathode)   += Imos + Imult   +        d_by_dt(Qds)
    i(emitter - > cathode) += Icss           +  Ccer * dVecdt
    i(emitter - > drain)   += Ibss           +        d_by_dt(Q)
    i(anode - > emitter)   += Vae/Rb

    dVdgdt :  dVdgdt= d_by_dt(Vdg)
    dVecdt :  dVecdt= d_by_dt(Vec)
    Q      :  Vebq=Veb

    Nsat   :  Nsat=Ic/(q*A*vpsat) - Imos/(q*A*vnsat)
    mucinv :  mucinv = Pm*log( 1. + alpha2/Pm**(2./3.) )/alpha1

    p(tnode)  -= power
    }
```

(a



(b

Fig. 4. a) Equations section of Saber IGBT electro-thermal template, and b) schematic of components of current and dissipated power within IGBT electro-thermal model.

IV. Thermal Network Component Models

In the new electro-thermal network simulation methodology, the thermal network is represented as an interconnection of thermal component models where each component represents an indivisible building block used by the designer to form the thermal network (see Fig.1). Figure 5 is a diagram of the structure of the thermal component models, indicating that the thermal component models interact with the external thermal network through thermal terminals. The terminals of the thermal component can be connected to the thermal terminals of other thermal component models, to the thermal terminals of electro-thermal models, and to thermal element models such as temperature sources. To use the thermal component models, the designer only needs to specify the connection points of the thermal terminals within the thermal network and the structural and material parameters of the model. The thermal component models are parameterized in terms of structural and material parameters so that the details of the heat transport physics are transparent to the user.

The thermal component models are based upon a discretization of the heat diffusion equation for various three-dimensional coordinate system symmetry conditions and include the nonlinear thermal conductivity of silicon and nonlinear convection heat transfer. A logarithmic grid spacing is used by the thermal component models to provide the high resolution needed near the heat sources for high power dissipation levels without resulting in an excessive number of thermal nodes. As indicated in Fig. 5, the user-defined structural and material parameters are used by the model to determine the optimized thermal grid for the discretization as well as the appropriate discretization coefficients. This results in both accurate and computationally efficient (compact) thermal models that are suitable for simulation of large electro-thermal networks. The thermal models also provide an output list of internally calculated parameters such as the thermal node positions that are useful for interpreting the simulated temperature waveforms.

The three-dimensional heat diffusion equation for isotropic materials (thermal conductivity is independent of direction) can be written as:

$$\nabla \cdot (k(T)\nabla T) = \rho c \frac{\partial T}{\partial t} \qquad (1a)$$

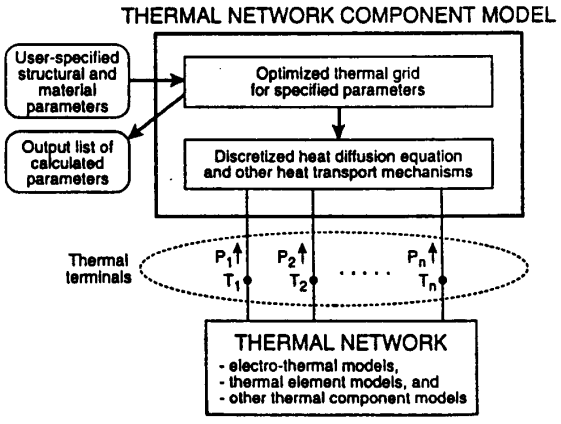


Fig. 5. Diagram of the structure of the thermal component models.

where the thermal conductivity is nonlinear for silicon and is given by [9]:

$$k(T) = 1.5486 \cdot (300/T)^{4/3}. \tag{1b}$$

For various symmetry conditions, this partial differential equation can be discretized into a finite number of first-order ordinary differential equations of the form

$$\frac{T_{i+1} - T_i}{R_{i,i+1}} - \frac{T_i - T_{i-1}}{R_{i-1,i}} = \frac{dH_i}{dt}, \tag{2a}$$

where

$$H_i = C_i \cdot T_i \tag{2b}$$

is the heat energy stored at thermal node i. The heat equation and the discretization coefficients ($R_{i,i+1}$, and C_i) are given in Table 3 for the rectangular coordinate system with y- and z-axis symmetry, Table 4 for the cylindrical coordinate system with z and θ symmetry, and Table 5 for the spherical coordinate system with θ and ϕ symmetry. The discretization coefficients are obtained by integrating the heat diffusion equations across the thermal element represented by each node (e.g., between $(x_{i-1} + x_i)/2$ and $(x_i + x_{i+1})/2$ for node i in rectangular coordinates), and by then applying finite differences to evaluate the spatial derivatives.

To implement thermal component models into Saber templates, the models are formulated such that the components of power flow between the thermal nodes are expressed in terms of the node temperatures. An example equations section for the discretized form of the heat diffusion equation is shown in Fig. 6. The first six statements of Fig. 6 describe the heat conduction between adjacent nodes using the thermal resistances (left-hand side of eq. (2a)). The last five statements describe the components of power stored as heat energy in the thermal capacitance at each thermal node (right-hand side of eq. (2a)). The discretized heat diffusion equation has a similar form for all of the thermal component models except that each model uses a different method to calculate the discretization coefficients.

For example, the silicon chip thermal model is based upon the rectangular coordinate heat diffusion equation and includes the nonlinear thermal conductivity of silicon. The parameters of the chip_therm template described in the netlist of Fig. 2b are the chip area a_chip and the chip thickness thick. Using these parameter values, the template calculates the positions of the internal nodes x_i to form the logarithmic grid spacing. The node positions, the chip area, and the instantaneous node temperatures are used to evaluate the model functions $R_{i,i+1}, C_i$, and H_i that are used by the equations section (Fig. 6). The node positions and heat capacitances are calculated in the parameters section of the Saber template prior to simulation time because they do not depend on simulator system variables. These calculated parameters can be listed when the templates are loaded by setting the parameter list > 0.

```
equations {
        p(junct -> node1)      +=    (Tj-T1)/Rj1
        p(node1 -> node2)      +=    (T1-T2)/R12
        p(node2 -> node3)      +=    (T2-T3)/R23
        p(node3 -> node4)      +=    (T3-T4)/R34
        p(node4 -> node5)      +=    (T4-T5)/R45
        p(node5 -> header)     +=    (T5-Th)/R5h

        p(node1)               +=    d_by_dt(H1)
        p(node2)               +=    d_by_dt(H2)
        p(node3)               +=    d_by_dt(H3)
        p(node4)               +=    d_by_dt(H4)
        p(node5)               +=    d_by_dt(H5)
        }
```

Fig. 6. Equations section for discretized form of heat diffusion equation.

The package models describe the two-dimensional lateral heat spreading, the die attachment thermal resistance, and the heat capacity of the periphery of the package. The lateral heat spreading in the package results in an effective heat flow area that increases with depth into the package. In the model, the effective heat flow area at each depth into the package is obtained by combining the components of heat flow area due to cylindrical heat spreading along the edges of the chip, the spherical heat spreading at the corners of the chip, and the rectangular coordinate component of heat flow directly beneath the chip.

TABLE 3
Rectangular Coordinate y- and z-axis symmetry

$$A\frac{\partial}{\partial x}\left(k(T)\frac{\partial T}{\partial x}\right) = A\rho c\frac{\partial T}{\partial t} \tag{T3.1}$$

$$C_i = A\rho c \cdot (x_{i+1} - x_{i-1})/2 \tag{T3.2}$$

$$R_{i,i+1} = (x_{i+1} - x_i)/A/k_{i,i+1} \tag{T3.3}$$

TABLE 4
Cylindrical Coordinate z and θ symmetry

$$A\frac{1}{r}\frac{\partial}{\partial r}\left(k(T)r\frac{\partial T}{\partial r}\right) = A\rho c\frac{\partial T}{\partial t} \tag{T4.1}$$

$$A = 2\pi r\gamma z \tag{T4.2}$$

$$C_i = \pi\gamma z\rho c\left[\left(\frac{r_{i+1} + r_i}{2}\right)^2 - \left(\frac{r_i + r_{i-1}}{2}\right)^2\right] \tag{T4.3}$$

$$R_{i,i+1} = \frac{1}{2\pi\gamma z k_{i,i+1}}\ln\left(\frac{r_{i+1}}{r_i}\right) \tag{T4.4}$$

TABLE 5
Spherical Coordinate θ and ϕ symmetry

$$A\frac{1}{r^2}\frac{\partial}{\partial r}\left(k(T)r^2\frac{\partial T}{\partial r}\right) = A\rho c\frac{\partial T}{\partial t} \tag{T5.1}$$

$$A = 4\pi r^2\gamma \tag{T5.2}$$

$$C_i = \frac{4}{3}\pi\gamma\rho c\left[\left(\frac{r_{i+1} + r_i}{2}\right)^3 - \left(\frac{r_i + r_{i-1}}{2}\right)^3\right] \tag{T5.3}$$

$$R_{i,i+1} = \frac{1}{4\pi\gamma k_{i,i+1}}\left(\frac{1}{r_i} - \frac{1}{r_{i+1}}\right) \tag{T5.4}$$

However, the lateral heat spreading does not extend beyond the edge of the package, so the distance that the heat spreads in each direction is limited in the model by the distance from each edge of the chip to the edges of the package. The effective heat flow area and the discretization coefficients are calculated internally by the model when the model templates are loaded, so the user only needs to specify the structural parameters such as the chip area, the location of chip on the package, and the package thickness to describe the lateral heat spreading.

The heatsink models describe the heat spreading at the heatsink package interface, the semi-cylindrical heat flow from the package toward the heatsink fins, and the nonlinear forced and natural convection heat transfer at the heatsink fins. The value of the effective heat flow area at the package-heatsink interface is determined by the package model and is used as a parameter for the heatsink models (a_heat of Fig. 2b). This parameter is used in calculating the heat spreading in the heatsink directly beneath the package and in determining the size of the grid spacing in the heatsink. For larger distances from the package within the heatsink, the heat flow becomes semi-cylindrical as the heat flows toward the heatsink fins. At the heatsink fins the heat is transferred to the ambient terminal by forced and natural convection.

The natural convection thermal resistance is given by [10]:

$$h'_{nat} = 4.84 \times 10^{-4} \frac{A_{fin}}{P_{fin}^{0.35}} \tag{3a}$$

$$R_{nat} = \frac{1}{h'_{nat} \cdot (T_f - T_a)^{0.35}} \tag{3b}$$

and the forced convection thermal resistance is given by:

$$f = \begin{cases} 1.7 + 0.148 \cdot \ln(v_{air}/508) & \text{for } v_{air} \le 508 \text{ cm/s} \\ 1.7 + 0.433 \cdot \ln(v_{air}/508) & \text{for } v_{air} > 508 \text{ cm/s} \end{cases} \tag{4a}$$

$$h'_{for} = f \cdot 4.88 \times 10^{-4} \frac{A_{fin}}{\sqrt{Z_{fin}}}, \tag{4b}$$

$$R_{for} = \frac{1}{h'_{for} \cdot \sqrt{v_{air}}} \tag{4c}$$

where the fin-to-ambient thermal resistance is the parallel combination of the forced convection thermal resistance, the natural convection thermal resistance, and the shunt mounting thermal resistance. Because h'_{nat} and h'_{for} do not depend upon the simulator system variables, they are calculated in the parameters section of the Saber template and can be listed when the templates are loaded.

V. Electro–Thermal Simulation Results

The new electro-thermal network simulation methodology provides the capability to incorporate thermal management considerations into the design of electronic systems. The electro-thermal semiconductor models can be used to predict the temperature-dependence of the semiconductor device characteristics for user-defined bias or transient conditions. The thermal network component models can be used to predict the transient thermal response of a user-defined thermal network topology for user-defined power dissipation functions. Finally, the electro-thermal semiconductor models can be combined with the thermal network component models to predict the interaction of the electrical and thermal networks. In this section, example electro-thermal simulations are given, and the results are verified by comparison with measurements. The temperature waveforms are verified using several different temperature measurement methods: 1) infrared microradiometer measurement of chip surface temperature waveforms [11,12], 2) thermocouple probe measurements of heatsink temperature waveforms, 3) three-dimensional transient finite element simulations of temperature [13], and 4) device temperature-sensitive electrical parameter measurements [11,12].

The temperature dependence of semiconductor device electrical characteristics varies with device part number as well as bias conditions or transient operating conditions. Therefore, semiconductor device data sheets cannot describe the temperature dependence for all of the applicable operating conditions. However, the electro-thermal semiconductor models discussed in this work can be used to describe the temperature dependence of a given device part number for user-defined bias conditions or transient operating conditions. For example, Figs. 7 and 8 compare the measured and simulated temperature dependence

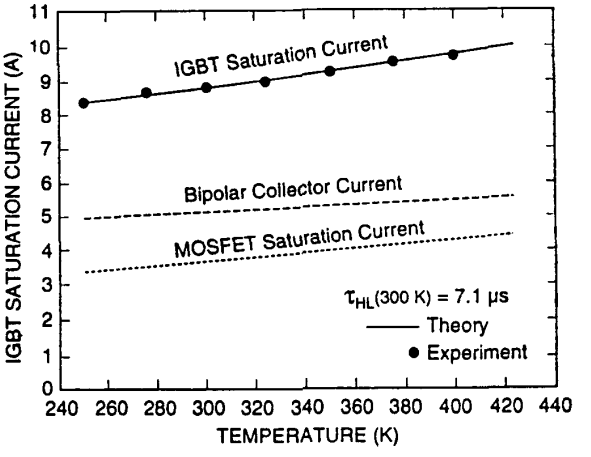


Fig. 7. Simulated and measured temperature dependence of IGBT saturation current for V_{ge} = 9 V and V_a = 10 V.

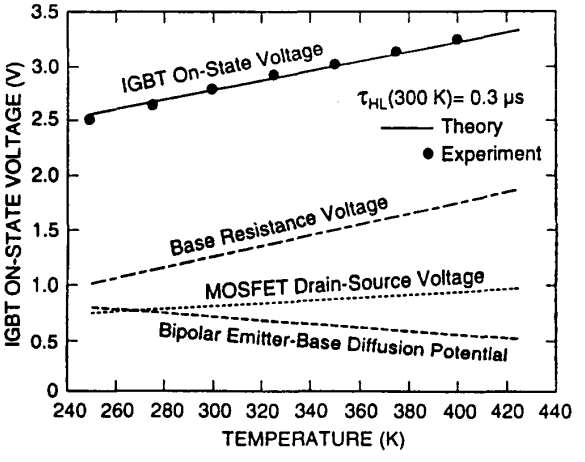


Fig. 8. Simulated and measured temperature dependence of IGBT on-state voltage for V_{ge} = 20 V and I_T = 10 A.

of the IGBT saturation current and on-state voltage characteristics for specific device types and bias conditions. The saturation current of Fig. 7 increases with temperature, but for higher currents or lower transconductance IGBTs, the saturation current decreases with temperature. The on-state voltage of Fig. 8 increases with temperature, but for IGBTs with higher base lifetimes or for lower anode currents, the on-state voltage can decrease with temperature. The simulations of Figs. 7 and 8 are performed using the Saber dc transfer analysis to sweep the ambient temperature source T_a which is connected directly to the IGBT thermal terminal. For transient conditions, a family of waveforms each for a different temperature can be generated using a Saber vary loop to step the device temperature.

Traditional methods for simulating the transient temperature distribution in semiconductor devices and packages are not suitable for simulating large thermal networks because they do not result in compact models that are both accurate and computationally efficient [7]. However, the new thermal network component models can be used to simulate the transient thermal response of user-defined thermal networks for user-defined power dissipation functions. For example, Fig. 9 compares the thermal step response predicted by the thermal component models with three-dimensional finite element simulations [13] for a) a 0.3-cm^2 area chip and b) a 0.1-cm^2 area chip in a TO247 package, where the temperature waveforms at various positions in the chip (0 through 500 μm) and the TO247 package (500 through 2500 μm) are indicated. The temperature drop in the package (T_h – 300 K) is larger for the large chip area (Fig. 9a) than for the smaller chip area (Fig. 9b) at the same power per unit area 1000 W/cm^2. This occurs because the lateral heat spreading in the package is more significant for the smaller chip and because the smaller chip is located farther from the edge of the package. The package model accounts for these effects, while the user only needs to specify the dimensions and location of the chip on the package.

Finally, the interaction of the electrical and thermal networks are described for different circuit operating conditions. For electro-thermal simulations, the instantaneous power dissipation determined by the electrical model is used by the thermal network to determine the evolution of the chip surface temperature. As the chip surface temperature changes, the electrical characteristics and power dissipation also change. Figure 10 shows an electro-thermal simulation for an IGBT short circuit condition, and Fig. 11 shows the thermal drift of the IGBT on-state voltage. The short circuit current of Fig. 10 increases with time because the saturation current increases with temperature (Fig. 7). The on-state voltage of Fig. 11 increases with time because the on-state voltage increases with temperature (Fig. 8). Because the temperature dependencies of the saturation current and on-state voltage have been verified for known chip temperatures (Figs. 7 and 8), the agreement between the simulated and measured electrical waveforms in Figs. 10 and 11 verify that the surface temperature waveforms are simulated accurately.

The heating of the thermal network is a non-quasi-static process so that the shape of the transient temperature distribution within the thermal network depends upon the power dissipation level. For the high-power dissipation level of Fig. 10 (1800 W/0.1-cm^2 chip area), only the top 150 μm of the silicon chip are heated during the transient condition and only 180 mJ of dissipated energy results in a 140 K rise in chip surface temperature at the end of the 100-μs short circuit pulse. However, for the relatively low power dissipation level of Fig. 11 (28 W/0.1-cm^2 chip area), the heat diffuses throughout the thermal network in the 500-s on-state condition, and several kJ of dissi-

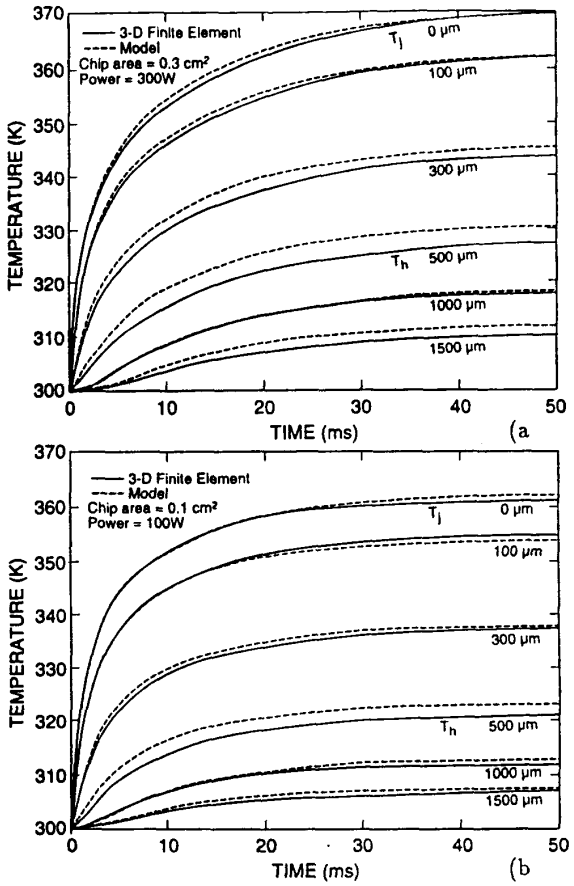


Fig. 9. Comparison of the thermal step response predicted by the thermal network component models with three-dimensional finite element simulations for a) a 0.3-cm^2 area chip and b) a 0.1-cm^2 area chip in a TO247 package, where the temperature waveforms at various positions in the chip (0 through 500 μm) and the TO247 package (500 through 2500 μm) are indicated.

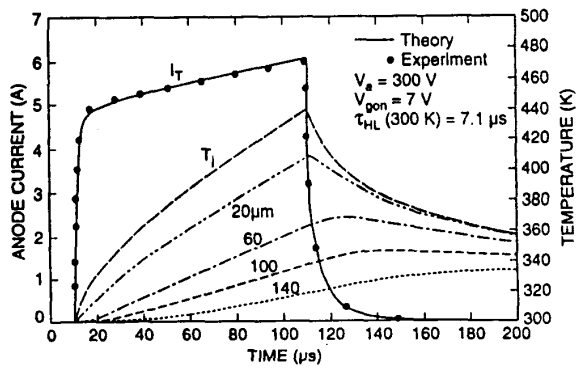


Fig 10. Simulated and measured IGBT short circuit current and simulated temperature waveforms at selected positions within silicon chip.

pated power are required to heat the chip surface to 80 K above the ambient temperature. The logarithmically spaced grid of the thermal models accurately describes the heating process for the full range of applicable power dissipation levels so that the user does not need to specify a different thermal grid for the different thermal heating conditions. If one were to assume a quasi-static model for the silicon chip such as a single thermal resistor and thermal capacitor, the predicted chip temperature of Fig. 10 would be a factor of five smaller than the actual temperature.

VI. Discussion of Computation Efficiency

The goal of the new methodology described in this paper is to produce accurate and computationally efficient (compact) models that are suitable for simulating large electro-thermal networks. Several aspects of the new methodology such as the principle of logarithmic grid spacing and the use of symmetry conditions to account for three-dimensional heat flow are essential for practical electro-thermal simulation. Without these innovations, the types of simulations demonstrated in Figs. 9 through 11 would not be practical due to the wide range of time constants of electro-thermal systems and due to the wide range of power dissipation levels that are applicable for the semiconductor devices. The primary factors that contribute to numerical complexity and reduce simulation speed are: 1) the number of simulator system variables that must be iterated by the simulator to solve the nonlinear model equations, 2) the degree of nonlinearity of the model functions, and 3) the relative time constants associated with simulator state variables that are integrated for transient simulation.

The heating of the thermal network is a non-quasi-static process, and a discretized heat equation with a wide range of time constants is required to describe the temperature distribution for the full range of applicable power dissipation levels. In the discretization process of eq (2), it is assumed that the temperature gradient and thermal conductivity do not vary substantially between adjacent thermal nodes. Therefore, the accuracy of the thermal component models is determined by the number and locations of the thermal nodes within the component. For high power dissipation levels during short periods

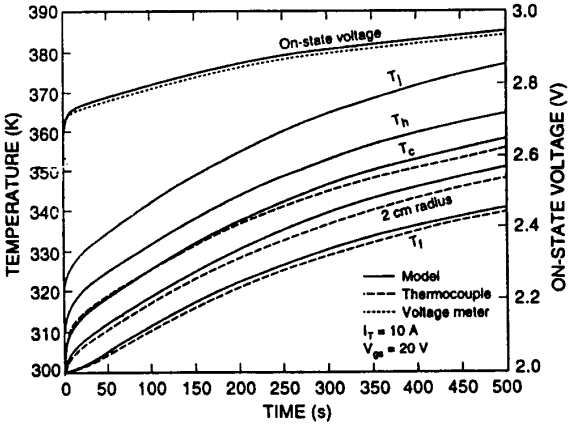


Fig. 11. Simulated and measured thermal drift of the IGBT on-state voltage where the temperature waveforms are measured using thermo-couple probes at the package-heatsink interface (T_c), a 2-cm radius from the package within the heatsink, and at the heatsink fins (T_f).

of time (e.g., for switching transients), the surface temperature rises faster than the heat diffuses into the chip (non-quasi-static heating), and a high density of thermal nodes is required at the silicon chip surface. However, the thermal gradients disperse as the heat diffuses through the thermal network, so a grid spacing that increases logarithmically with distance from the heat source (silicon chip surface) results in the minimum number of thermal nodes required to describe the temperature distribution for the range of applicable power dissipation levels.

In general, a discretization approach for solving a partial differential equation results in a larger number of system variables (one for each node) with small time constants associated with each node (proportional to the inverse square of the number of nodes). However, the logarithmic grid spacing principle and the use of symmetry conditions reduces the number of nodes required by the thermal models by several orders of magnitude. In addition, thermal time constants are much longer than electrical time constants, so the discretized heat equation does not result in fast time constants that reduce simulation speed. Whereas if a discretization approach were used to solve the semiconductor device electrical equations, the discretization time constants would become the fastest time constants of the system and would slow the simulation speed dramatically. Finally, the nonlinearities for the thermal network are generally weak functions of temperature. As a consequence, the simulation CPU times of the new electro-thermal network simulation methodology are comparable to those of the corresponding electrical network, not including thermal network.

Although the electro-thermal CPU times are comparable to those of the corresponding electrical network, the simulation intervals required to describe thermal phenomena such as the thermal drift of Fig. 11 can be as long as several minutes, whereas typical simulation intervals for electronic circuits are several milliseconds. Because the electro-thermal networks have time constants that range from nanoseconds to kiloseconds, the class of problems that result in practical simulation times is limited. For example, in the simulation of Fig. 11, the fast time constants of the semiconductor device are not activated, and the simulation CPU time is less that 1 min on a Sun SparcStation 2. However, if one were to simulate the same circuit but with a 20-kHz switching frequency, millions of switching cycles would occur during the 500-s simulation interval and the simulation CPU time would be much longer. When simulating electro-thermal phenomena which require long simulation intervals, the user must be careful not to activate fast time constants that are unnecessary for the understanding of the circuit. The long electro-thermal simulation intervals can also be reduced by using a thermal simulation with an average power dissipation to set the initial conditions of the thermal network temperatures before the high frequency electro-thermal simulation begins.

VII. Conclusions

A new circuit simulation methodology has been developed in which the temperature used by the electro-thermal semiconductor device models is determined by the simulator. The electro-thermal models are developed using physics-based semiconductor models, the temperature-dependent properties of silicon, and the extracted temperature dependence of the model parameters. The power dissipated in the semiconductor devices is used by the thermal network models to determine the dynamic temperature distribution within the thermal network, where the thermal network is represented by an interconnection of thermal components so that different thermal network topologies can readily be examined. The thermal components are param-

eterized in terms of structural and material parameters so that the details of the heat transport physics are transparent to the user. A systematic procedure has been presented for developing both the electro-thermal semiconductor models and the thermal network component models. The electro-thermal network simulations are useful for determining 1) the temperature dependence of semiconductor device electrical characteristics for user-defined operating conditions, 2) the response of thermal networks to user-defined power dissipation functions, and 3) the interaction of electrical and thermal networks.

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Nomenclature *

A	Device active area, heat flow area (cm^2).
A_{fin}	Total heatsink fin area (cm^2).
BV_b	Junction break-down voltage coefficient.
c	Specific heat (J/cm·K).
C_i	Thermal capacitance of node i (J/K).
C_{cer}	Collector-emitter redistribution capacitance (F).
C_{gd}	Nonlinear gate-drain capacitance (F).
D_n, D_p	Electron, hole diffusivity (cm^2/s).
f	Forced convection correction factor.
H_i	Heat energy at node i (J).
h'_{for}	Forced convection heat transfer coefficients.
h'_{nat}	Natural convection heat transfer coefficients.
i	Discretization indices.
I_{bss}	Charge control base current (A).
I_c	Collector current (A).
I_{ccer}	Collector-emitter redistribution current (A).
I_{css}	Charge control collector current (A).
I_{mos}	MOSFET channel current (A).
I_{mult}	Multiplication current (A).
I_{snc}	Emitter electron saturation current (A).
I_T	Anode current (A).
k	Boltzmann's constant (J/K).
$k(T)$	Thermal conductivity (W/cm·K).
$k_{i,i+1}$	$k(T)$ between nodes i and $i+1$ (W/cm· K).
K_p	MOSFET transconductance parameter (A/V^2).
n_i	Base intrinsic carrier concentration (cm^{-3}).
P_{fin}	Heatsink fin height, orientation parameter (cm).
Power	Total dissipated power (W).
Q_{gs}	Gate-source capacitance charge (C).
Q_{ds}	Nonlinear drain-source capacitor charge (C).
Q	Bipolar transistor base charge (C).
R_b	Conductivity modulated base resistance (Ω).
R_{for}	Forced convection thermal resistance (K/W).
R_g	Gate drive resistance (Ω).
$R_{i,i+1}$	Thermal resistance between x_i and x_{i+1} (K/W).
R_{nat}	Natural convection thermal resistance (K/W).
r_i	Cylindrical, spherical radius of node i (cm).
T_0	Reference temperature (K).
T_a	Ambient temperature (K).
T_c	Package case temperature (K).
T_f	Heatsink fin temperature (K).
T_h	Package header temperature (K).
T_i	Temperature at node i (K).
T_j	Silicon chip surface temperature (K).
V_a	Anode-cathode voltage (V).
V_{aa}	Anode supply voltage (V).
V_{ac}	Voltage across R_b (V).
V_{gs}	Gate-source voltage (V).
V_T	MOSFET threshold voltage (V).
v_{air}	Forced convection air velocity (cm/s).
v_{nsat}, v_{psat}	Electron, hole saturation velocity (cm/s).
x_i	Position of node i (cm).
Z_{fin}	Height of heatsink fin (cm).
α_1, α_2	Carrier-carrier scattering coefficients.
$\beta_{tr,v}$	Relative size of current tail.
γ	Cylindrical, spherical angle fraction.
τ_{HL}	High-level injection lifetime (s).
ρ	Mass density (g/cm^3).
μ_n, μ_p	Electron, hole mobility ($cm^2/V{\cdot}s$).

* Model parameters with subscript 1 represent temperature coefficients and the sans serif symbols represent computer mnemonics.