Analysis of Conducted EMI Emissions from PWM Inverter Based on Empirical Models and Comparative Experiments

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ABSTRACT—**For the purpose of investigation of electromagnetic interference (EMI) mechanisms in PWM inverter, empirical models and comparative experiments were studied in both time-domain and frequency-domain. Models of the major circuit components including switching devices, passive components and interconnects were obtained with physics-based device modeling and time-domain reflectometry (TDR) for parasitics characterization. A full-bridge inverter was then constructed with all empirical models included to study the fundamental mechanisms by which the EMI noises are excited and propagated. With separation of common- and differential-mode EMIs, the simulation results were compared with actual experiments to examine the significant roles of parasitic elements coupled with device switching dynamics in EMI generations.**

I. INTRODUCTION

It is typical today that ac motor drives require fast switching transitions and high switching frequencies of the voltage-source PWM inverters to achieve high performances in dynamic response, efficiency, acoustic noise, size, and weight. The emergence of high-speed switching devices such as the insulated gate bipolar transistor (IGBT) has enabled an increase in inverter switching frequencies and thus led to much improvement of inverter operating characteristics. However, these fast switching inverters generate high voltage slew rate (*dv/dt*) and high common-mode voltage at motor terminals, causing some serious problems, such as premature winding failure, ground leakage current, shaft voltage and bearing current, and conducted and/or radiated electromagnetic interference (EMI) [1-4].

Many recent research papers have addressed the problems that high-speed switching devices have imposed on PWM drive applications. High *dv/dt* may result in premature insulation failure resulting in the failure of inductor, motor, or transformer. High *dv/dt* is also largely responsible for conducted EMI as identified in [5-10].

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In recent years, EMI considerations have become increasingly important, as the electromagnetic compatibility (EMC) regulations (typically defined from 10 kHz to 30 MHz) have become more stringent. It is commonly realized that the high switching *dv/dt* and *di/dt* are the main sources of EMI noise. The higher switching *dv/dt* or *di/dt*, the higher EMI emissions. However, a PWM drive system is very complicated in terms of the power stage, control circuit, and external connections. While some EMI phenomena have been described and some useful conclusions drawn in recent studies, the fundamental mechanisms by which the EMI noises are excited and propagated have not been adequately investigated.

An essential part of such EMI study is the modeling of device switching dynamic behavior and identification and characterization of various parasitic components within the PWM inverter system. In this paper, a physics-based IGBT model developed by Hefner [11-13] is chosen for obtaining correct switching waveforms with high-frequency effects such as *dv/dt* and current tailing. The device model parameters were extracted with experiments. The parasitic components were measured with time-domain reflectometry (TDR) method [14].

The inverter circuit model is then constructed with major parasitic inductance and capacitance in device modules, passive components, leads, and interconnects. To verify the validity of the inverter model, a comparative study is performed with computer simulations and hardware experiments on a 50-kW full-bridge IGBT inverter prototype. Moreover, the fundamental mechanisms by which the EMI noises are excited and propagated are analyzed with separation of common-mode (CM) and differential-mode (DM) EMIs, and the significant roles of parasitic elements coupled with device switching dynamics in EMI generations are examined.

II. PROTOTYPE INVERTER AND TEST SETUP

Although the study of a three-phase inverter is more desirable, a full-bridge one should have similar features of the basic EMI mechanism. Especially, the analysis of the simplified case can ease the identification of the basic EMI

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production mechanism, and the results can be extended to three-phase inverter. Figure 1 shows the circuit of a full-bridge IGBT based inverter. The prototype inverter is designed to have a rating of 50 kW at 300-V dc bus voltage. The switch pairs S1-S4 and S2-S3 are half-bridge IGBT modules rated at 600 V/400 A.

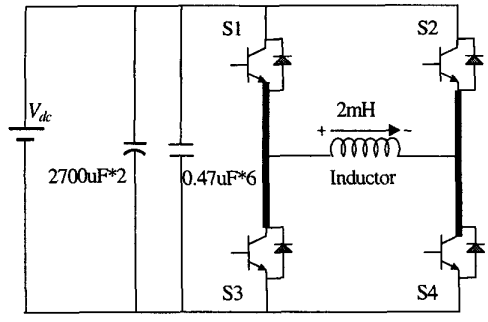


Fig. 1. Circuit diagram of the single-phase full-bridge inverter

The PWM control signal is generated by comparing a sinusoidal reference signal with a 20-kHz triangular carrier signal. Since EMI is closely related to layout and interconnects, a custom-made laminated bus bar is adopted to reduce interconnect parasitics. Two bulk capacitors with 2700 μF each are connected on the two ends of the laminated bus bar. Six high frequency polypropylene capacitors are mounted directly on top of the bus bar to reduce the interconnect inductance.

The connection of the prototype inverter along with the load and two line-impedance-stabilizing-networks (LISNs) is shown in Fig. 2. As required by EMC regulations, a large ground reference plane is used as the reference earth ground. Each LISN provides 50-Ω impedance to the system under test. It also prevents the noise in the source from entering the system under test. For safety reasons, the load frame and the inverter heatsink are grounded, as indicated by the connections to the ground reference plane in Fig. 2. Conducted EMI measurements are made by observing the voltage developed across the defined LISN impedance with a spectrum analyzer. With this configuration, the total EMI noise can be measured on any one of the LISN impedance, while the CM or DM EMIs can be separated by taking the sum or difference, respectively, of the voltage signals picked up by the two LISNs.

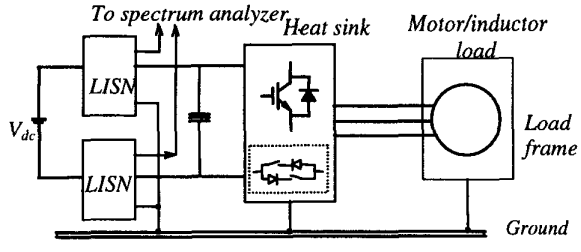


Fig. 2. Inverter and LISN connection for EMI measurement.

The EMI room and complete test setup is shown in Fig. 3. Because the purpose of the study is to analyze the source and propagation mechanism of EMI, the setup tends to allow ease of operation, but not to fully comply with EMC regulations. With most instruments inside the room, the background noise before starting the inverter was noticed and recorded for reference purpose.

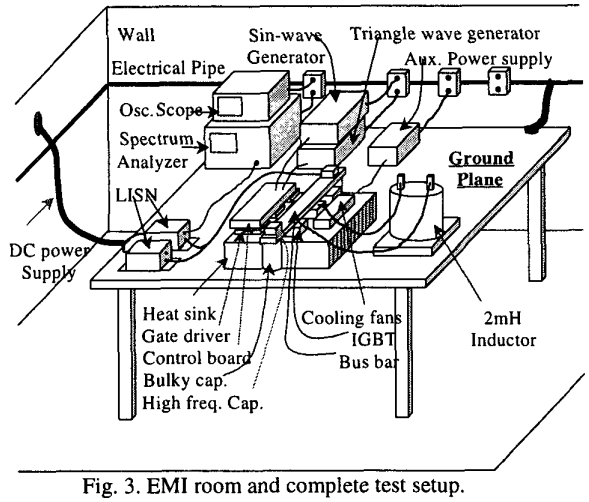


Fig. 3. EMI room and complete test setup.

III. Inverter Modeling

For the purpose of EMI performance evaluation and prediction, accurate circuit device and component models with good simulation tools are needed. The simulation allows the dominant high frequency current paths to be identified and the inverter design to be optimized. Models required in the simulation include the power devices, parasitic components of passive component, cables and interconnects, stray capacitors, and ground coupling.

A. *Device Model*

For an accurate power semiconductor device model, several effects need to be considered with high priority since they dominate the high-frequency switching characteristics. These effects have not been described correctly before because their influence on low-power devices is negligible. For high power IGBT devices, the important effects that need to be modeled are resistivity modulation, charge storage, MOS capacitances, electrothermal interaction, and breakdown phenomenon. Special challenges in developing such models for circuit simulation arise from the need to simultaneously fulfill contradicting requirements like high quantitative accuracy, low demand of computation power, and low demand of physical or structural or technological model parameters.

Recently, a physics-based IGBT model has been developed for the first time by Hefner and has become

available in the Saber† simulator [11-13]. The IGBT modeling work also provides a detailed parameter extraction method. Such an advanced IGBT model with high-frequency switching characteristics is necessary to obtain correct switching waveforms such as *dv/dt* and current tailing. The model parameters of the IGBT device used in the prototype inverters are extracted with experiments and are given in the appendix of this paper.

Various parasitics exist inside an IGBT module. The authors have proposed the use of TDR measurement for characterization of lead and interconnect parasitics in [14]. With TDR method, the lead and interconnect inductances in the IGBT module can be measured without intruding the device.

In addition to interconnect parasitic inductances, there are also parasitic capacitances between IGBT collectors and the module metal baseplate. These capacitances cause high-frequency leakage current flowing to the metal baseplate that is connected to the heatsink. The heat sink is normally grounded for safety reasons. The IGBT devices are mounted on the metal base plate with a thin electrical insulating material. To make the thermal resistance small, the insulating layer is normally made as thin as possible and the stray capacitance between the collector and the base plate tends to be large. With inclusion of interconnect inductance and the stray capacitance, the complete IGBT module equivalent circuit is shown in Fig. 4.

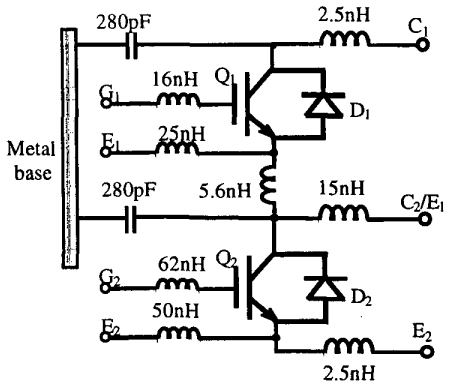


Fig. 4. Equivalent circuit of the IGBT module with interconnect inductance and stray capacitance.

B. *Parasitic Models of Bus Bar and Bulk Capacitor*

The custom-designed bus bar and the dc bulk capacitor used in the prototype inverter are characterized using the TDR method [14]. The bus bar is used to connect the dc power source to the three IGBT inverter output legs. The bus bar has three sets of bushings in the middle for connection to the IGBT modules, which divide the bus bar into four equal lengths, and thus the bus bar behaves like a transmission line with an average characteristic impedance of 1.5 Ω and a total time delay of 3.0 ns. As shown in Fig. 5, the transmission line model can be partitioned into four equal segments and approximated as four *LC* filters in series where L = 1.25 nH and C = 0.55 nF.

For the bulk capacitor, the parasitic component that affects EMI the most is the equivalent series inductance (ESL). With TDR measurement result, the ESL of a 450 V, 2700 μF electrolytic capacitor was found to be 15 nH.

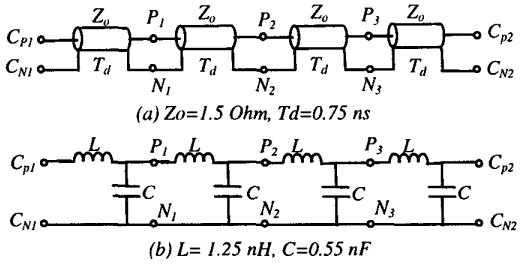


Fig. 5 Equivalent models of the busbar.

IV. Time Domain Comparative Study

The EMI production mechanism includes the noise source and the noise path. The noise source is related to the voltage and current rates of change, i.e., *dv/dt* and *di/dt*. These rates of change can be observed from time-domain study. With inclusion of major parasitic components and the use of physics-based device model, the simulated and experimental time-domain IGBT turn-on and turn-off voltage and current waveforms are shown in Figs. 6 and 7, respectively.

Because parasitics of the sensor connections and instrumentation probes are not included in the simulation model, some high-frequency oscillations shown in the experimental waveforms are not quite predicted in the simulation. However, both turn-on and turn-off voltage and current rates of change are well matched with the computer simulation. Although the additional parasitic components can alter the frequency-domain characteristic, their energy level is

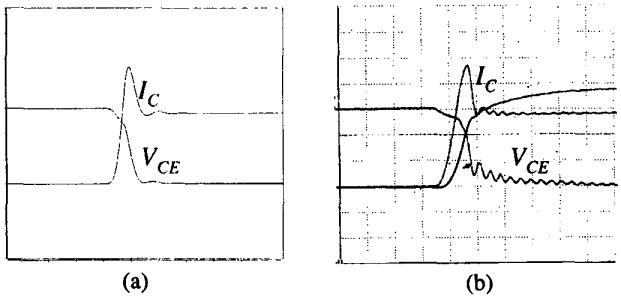
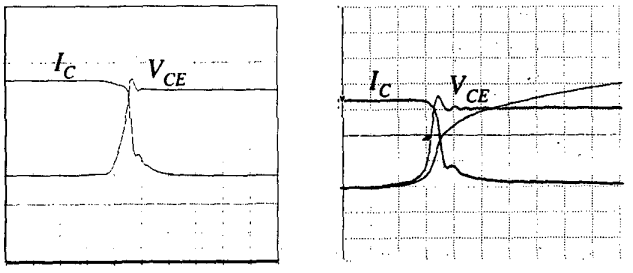


Fig. 6. IGBT turn-on waveforms (a) simulation, (b) experiment with V_{CE}: 100V/div, I_C: 40A/div, and Time: 200 ns/div.

† Certain commercial products are identified in this paper in order to specify the experimental procedure adequately. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that these products are the best available products for the purpose.



(a) (b)

Fig. 7. IGBT turn-off waveforms (a) simulation, (b) experiment with V_{CE}: 100V/div, I_C: 40A/div, and Time: 200 ns/div.

Low, and is better to be neglected for the study to avoid unnecessary complexity and difficulty of convergence in simulation process.

V. Frequency Domain Comparative Study

The inverter operation is simulated to obtain its EMI spectra using the developed circuit model with major parasitic inductance and capacitance in device modules, passive components, leads, and interconnects. The inverter simulation is in time domain, and the EMI spectra are then calculated from the time-domain noise voltage picked up by the LISNs using Fast Fourier Transformation (FFT). To verify the validity of the inverter model, comparative study is performed between simulations and experiments with the same inverter operating conditions.

Conducted EMI performance, traditionally studied from 10 kHz and 30 MHz, is normally examined with two different frequency ranges: (1) low frequency range (from 10 kHz to 150 kHz) and (2) high frequency range (from 150 kHz to 30 MHz). Figs. 8 and 9 show the comparison of the low-frequency EMI noise spectra between simulation and experimental results with separation of CM and DM noises from the total noises. Figs. 8(a), 8(b), and 8(c) are the simulated total, DM, and CM noise spectra, respectively; while shown in Figs. 9(a), 9(b) and 9(c) are the experimental counterparts.

As can be seen from Figs. 8 or 9, the EMI noises in the low frequency range have high peaks at the multiples of the 20-kHz switching frequency, and the DM noise is the dominant component as compared to the CM noise. From this low-frequency comparison, it can be seen that the simulation and experimental results match well except the high frequency components between these multiple peaks.

For the EMI comparison in the high frequency range, the simulation results of the total, DM, and CM noises are shown in Figs. 10(a), 10(b), and 10(c), respectively; while the experimental counterparts are shown in Figs. 11(a), 11(b) and 11(c), respectively. The inverter operating conditions for the shown EMI spectra are all the same at 300-V input voltage and 50-A rms load current with 100-Hz fundamental frequency.

In the high frequency range, the CM noise is more dominant than the DM noise, especially at frequencies higher than 10 MHz, as can be seen from Figs. 10 or 11. Comparing the simulation results shown in Figs. 10(a), 10(b), and 10(c) with the experimental counterparts shown in Figs. 11(a), 11(b), and 11(c), a fair matching (with less than 10-dB difference) can be observed at the frequencies lower than 10 MHz, but a mismatching can be seen at the frequencies higher than 10 MHz.

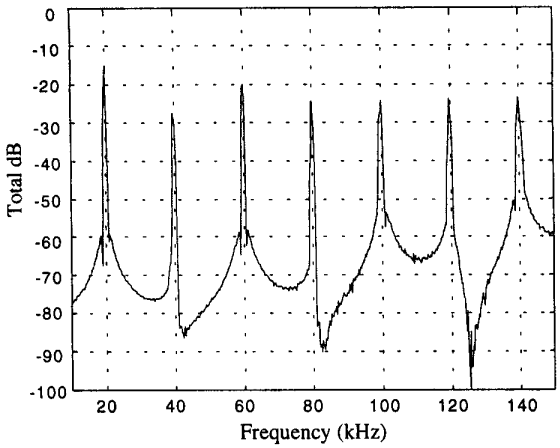
It should be noticed that in the comparison between Fig. 10(b) and Fig. 11(b), the DM noise spectra match quite well between simulation and experiment. In other words, the inclusion of all the parasitic components in the DM path is valid for low-frequency and some high-frequency portions especially below 10-MHz range. The IGBT model, which affects the effectiveness of the noise source, is also valid to a large extent. However, the parasitic components in the CM path are not modeled sufficiently in this paper.

The path of differential EMI mainly consists of parasitic inductance of device, bulk capacitor, and interconnects. The DM noise current flows through the inductor windings, and through the winding capacitance of the inductor, back to the power mains via the dc bus.

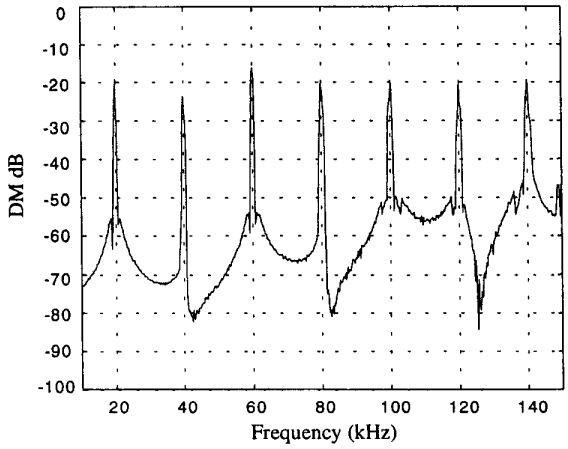
The common-mode noise current flows through the stray capacitance of the load inductor to the inductor frame and back to the source via the power mains. The common-mode current also flows through the stray capacitance between the IGBT collector and the module's baseplate that is normally grounded through the heatsink.

The mismatch in high frequency spectra can be considered as follows:

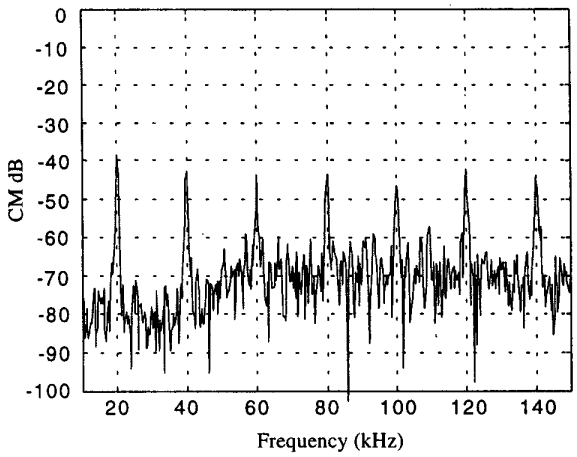
(1) The gate drive and gate drive power supply noises are not included. These noises contain mainly high frequency DM and CM noises [8].
(2) The CM path parasitic components are not included sufficiently. In the simulation, the only major CM path that is included is the parasitic capacitance between IGBT and heatsink. Other CM paths created by load, power supply transformers, opto-couplers, control circuit switchings, etc. were not included.
(3) The background EMI noises from instrumentation and their associated power supplies are neglected.
(4) The sampling and computational methods for spectrum analysis are different between simulation and experiment. The simulation takes limited sampling data and performs FFT only for one fundamental cycle. However, the experimental results contain significant amount of data, and its spectra are obtained from quasi-peak mode analysis.



(a) Simulated total spectrum in the low-frequency range.

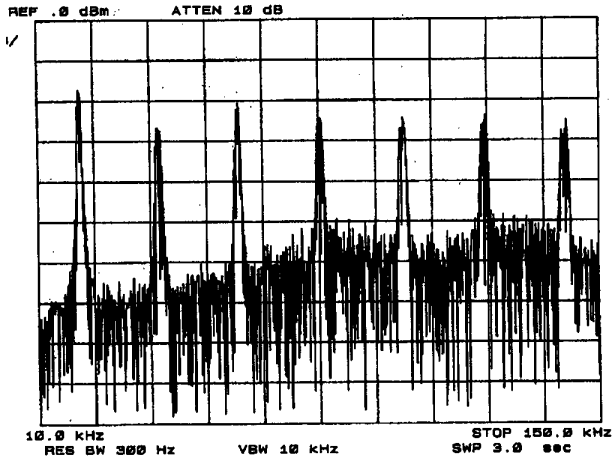


(b) Simulated DM spectrum in the low-frequency range.

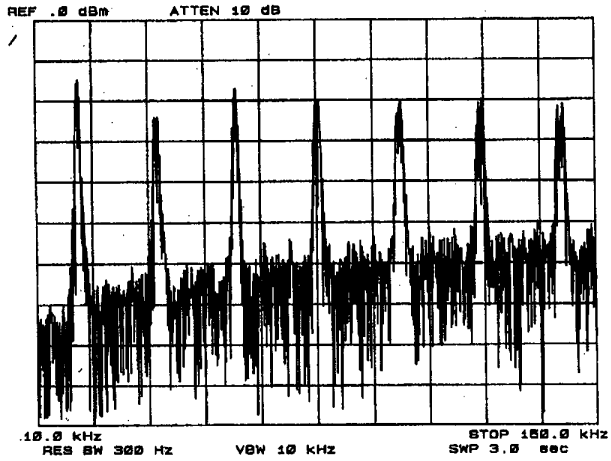


(c) Simulated CM spectrum in the low-frequency range.

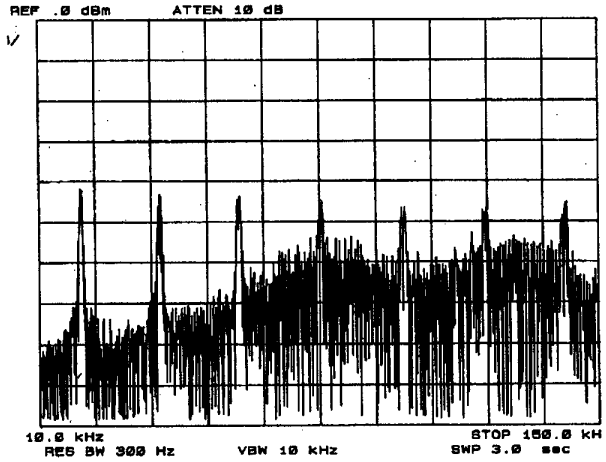
Fig. 8. Simulated EMI noise spectra in the low-frequency range for the 50-kW IGBT inverter.



(a) Experimental total spectrum in the low-frequency range.

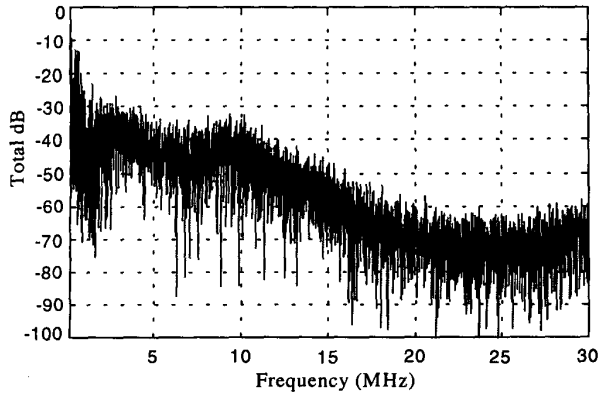


(b) Experimental DM spectrum in the low-frequency range.

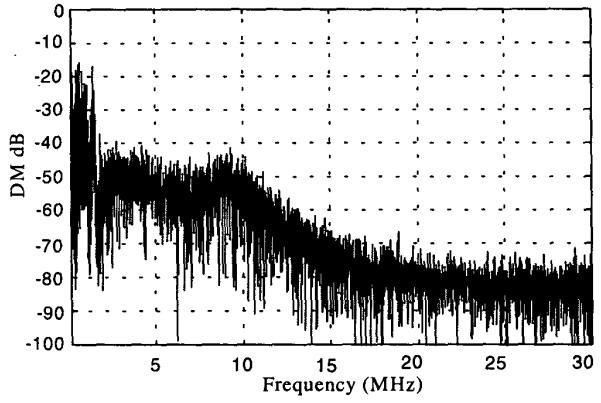


(c) Experimental CM spectrum in the low-frequency range.

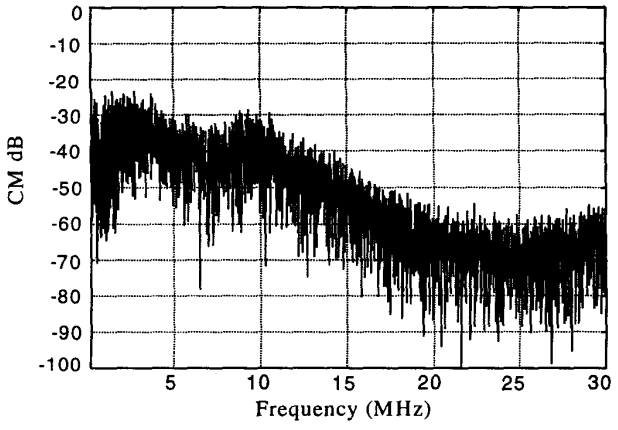
Fig. 9. Experimental EMI noise spectra in the low-frequency range for the 50-kW IGBT inverter.



(a) Simulated total spectrum in the high-frequency range.

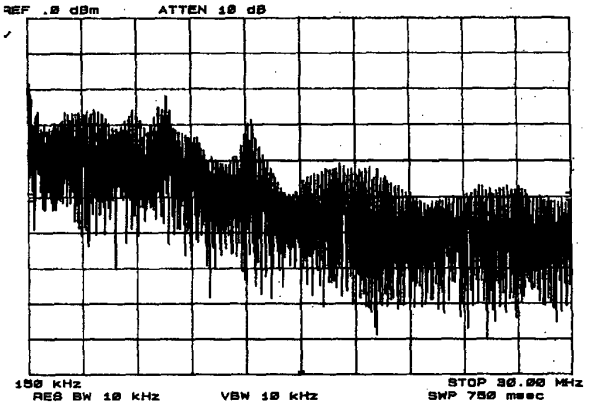


(b) Simulated DM spectrum in the high-frequency range.

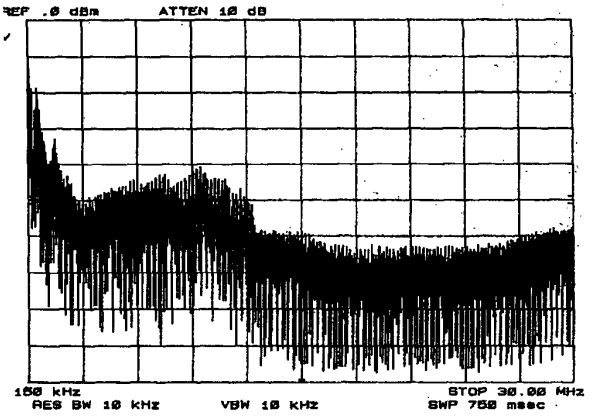


(c) Simulated CM spectrum in the high-frequency range.

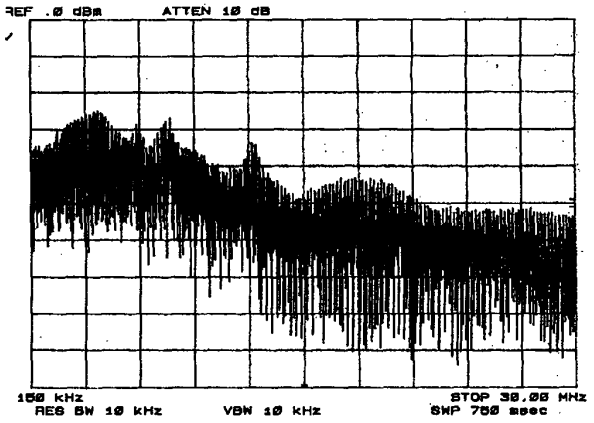
Fig. 10. Simulated EMI noise spectra in the high-frequency range for the 50 kW IGBT inverter.



(a) Experimental total spectrum in the high-frequency range.



(b) Experimental DM spectrum in the high-frequency range.



(c) Experimental CM spectrum in the high-frequency range.

Fig. 11. Experimental EMI noise spectra in the high-frequency range for the 50 kW IGBT inverter.

It is a common practice (as in our experiments) to connect capacitors with low equivalent series resistance (ESR) and low equivalent series inductance (ESL) across the dc bus as surge absorbers. These high quality capacitors provide a low-impedance path over a wide frequency range to absorb switching transients. The high-frequency DM noise current mainly flows through these dc bus capacitors instead of flowing through LISNs to the mains power supply. Thus, the DM noise current does not contribute much of the conducted EMI in the high frequency range, and the CM noise current is the dominant component of the total EMI emission in a PWM inverter system.

VI. Conclusion

With the use of empirical models and comparative studies between simulation and experiment, this paper presents a new way of EMI study. The fundamental mechanisms by which the EMI noises are excited and propagated are described clearly with separation of CM and DM noises. The match of low-frequency EMIs especially in the differential mode indicates that the proposed modeling approach with inclusion of noise sources and noise paths is effective. The physics-based device switching model, parasitics in device modules, passive components, leads, and interconnects used in this paper are also valid. However, there seems to be a long way to go for high frequency parasitic modeling and identification of CM noise sources. This paper has shown a satisfactory prediction for frequencies up to 150 kHz. The DM noise prediction is nearly acceptable below the 10 MHz range. It is expected that in a near future the prediction of entire EMI generation mechanism can be pushed up to 10 MHz.

Appendix

Table I. Model parameters of the IGBT device:

Symbol	Value	Description
A	3.6	Device active area (cm^3)
τ_{HL}	5.6E-7	High-level excess carrier lifetime (s)
I_{sne}	6E-13	Emitter electron saturation current (A)
W_B	6.7E-3	Metallurgical base width (cm)
N_B	1.0E14	Base doping concentration (cm^{-3})
W_{buf}	6.5E-4	Buffer layer width (cm)
τ_{buf}	3.25E-7	Buffer layer excess carrier lifetime (s)
N_{buf}	2.4E17	Buffer layer doping concentration(cm^{-3})
V_T	5.0	MOSFET channel threshold voltage (V)
K_p	56.9	MOSFET channel transconductance in saturation region (A/V^2)
K_f	2.0	Factor of K_p in triode region to that in saturation for MOSFET
C_{gs}	3.03E-8	Gate-source capacitance (F)
C_{oxd}	3.6E-8	Gate-drain oxide capacitance (F)
R_s	0.3	Intrinsic series resistance ($m\Omega$)
A_{gd}	1.8	Gate-drain overlap active area (cm^2)
V_{TD}	0	Gate-drain overlap depletion threshold voltage (V)

Acknowledgment

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