Development of Thin-Film Multijunction Thermal Converters at NIST*

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Abstract

This paper gives an overview of the development of thin-film multijunction thermal converters (FMJTCs) at the National Institute of Standards and Technology (NIST). A historical perspective of film thermal converters is presented, followed by descriptions of the motivation, fabrication processes, physical characteristics and the electrical properties of the FMJTCs produced at NIST. Integrated micropotentiometers which incorporate FMJTCs and thermal converters, produced by an alternative fabrication technology using a CMOS foundry, are also described. The paper concludes with a report on the current status of the FMJTC project and future directions.

Introduction

There has been considerable interest in the use of micromachining of silicon and photolithography on thin-films to produce various types of sensors. This paper describes the project at NIST to develop new MJTCs and related devices using those technologies. The goal was to produce MJTCs with performance comparable to conventional wire MJTCs in the audio-frequency region but with greater overall frequency and current ranges and at lower cost. Such new MJTCs could potentially be useful in commercial instruments as well as for laboratory standards. Several other projects or proposals to develop thin-film MJTCs had been reported when the NIST effort began in earnest in 1990 [1-4].

Construction

The basic elements of the FMJTCs are a thin-film heater supported on a thin dielectric membrane, a silicon frame surrounding the structure, and thin-film thermocouples positioned with hot junctions near the heater and cold junctions over the silicon [5]. The heater and thermocouples are sputter-deposited and photolithographically patterned. Photolithographic fabrication of thin-film MJTCs allows for accurate dimensioning of the heater and thermocouples. The planar design and the spacing between the thermocouples and the surrounding heatsink reduce the temperature variations along the heater in the region sampled by the hot junctions. Contributions to ac-dc difference from Thomson and other effects are further reduced by the appropriate choice of heater alloy.

The silicon frame provides a good heat sink for the thermocouple cold junctions and is mounted directly on an aluminum oxide substrate to provide an even more effective heat sink. To reduce the error due to Peltier effect, the contact pads for wire bonded leads are placed over the silicon frame. These thermal and physical design characteristics also contribute to very small dc reversal errors.

To provide mechanical stability and good thermal efficiency, a thin, multilayer membrane has been used to support the heater structure and the thermocouple hot junctions. Low overall stress and low dielectric loss have been achieved in the membrane by the fabrication of balanced layers of SiO_2 and Si_3N_4. The heater was placed on the membrane, without silicon underneath, to reduce the dielectric loss and therefore reduce the ac-dc difference and voltage or current coefficients. Low ac-dc difference, small dc reversal, and high thermal efficiency have been achieved by the thermal design, physical arrangement, and careful selection of materials for the heater and thermocouples.

Geometric Designs

Several different geometric designs have been developed incorporating variations in heater geometries and thermocouple positions. They include a linear heater which can be assembled in a coaxial geometry, a bifilar heater, and a short, wide heater designed for currents of 100 mA or higher. Some converters contain thermocouples adjacent to the heater while others have thermocouples that are located directly over the heater separated by a layer of SiO_2.

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Custom packages consisting of aluminum oxide substrates patterned with thick-film conductors have been designed and fabricated to provide long-term stability, small distributed capacitance and inductance, and minimum skineffect through the use of all non-magnetic materials. These packages preserve the inherent ac-dc differences of the thin-film MJTCs.

New integrated micropotentiometers have also been developed for this project [6]. They are used as millivolt and microvolt standards and contain thin-film MJTCs and thin-film output resistors fabricated as an integrated structure on the same silicon chip. Several different types of these devices have been made. Most were single-range versions with a 5 mA MJTC combined with either a 20 Ω, 2 Ω, or 0.2 Ω output resistor. Others were multirange devices with as many as five voltage ranges from 1 mV to 200 mV.

Performance

Representative results on the FMJTCs include ac-dc differences of sub-μV/V values at 1 kHz, a few μV/V or less from 50 kHz up to 100 kHz, and several tens of μV/V at 1 MHz for a bifilar-heater MJTC used as a voltage converter. The dc reversal errors are only a few μV/V or less, as expected. Various versions of the FMJTCs are usable up to 100 MHz. Several characteristics improve at lower pressures and lower temperatures. Output emf and the thermal time constant increase about eight times at 0.13 Pa making a more efficient converter and reducing the low-frequency ac-dc difference at 100 Hz and below. The large increase in efficiency at low pressure permits the use of vacuum mounted MJTCs at currents as low as 1 mA and voltages below 100 mV. For instrumentation applications, the FMJTCs are suitable for operation with output emfs as high as 0.5 V.

The ac-dc differences of the thin-film, integrated micropotentiometers are generally close to the presently available calibration uncertainty at audio-frequency but range up to several percent up to 100 MHz.

CMOS-foundry Design and Fabrication

The MJTCs described above require custom processing; however, MJTCs have also been fabricated using CMOS-foundry compatible micromachining [7,8]. The CMOS-foundry compatible micromachining technique is based on the incorporation of open areas in the mask layout that bares the silicon surface. After receipt from the foundry, the silicon under the open area is etched away leaving a pit and suspended structure. The technique used in this project permitted only layers of polysilicon and aluminum. These layers are encapsulated in SiO_2 that act both as the protective barrier to the etchant and as the mechanical support. The polysilicon heater resistor and the hot thermocouple junctions were suspended on a web or cantilever created by etching a pit in the silicon about 150 μm x 150 μm in area. The thermocouples are made of aluminum-polysilicon. The choice of materials limits the performance of these CMOS-foundry MJTCs; however they offer extremely small size, high output emf, very low cost, and the opportunity for easy inclusion with other circuitry for commercial applications.

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