PROGRESS TOWARD AN AC JOSEPHSON VOLTAGE STANDARD

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Abstract

Progress toward a Josephson voltage standard for fast dc measurements and ac waveform synthesis is described, including a version with SNS junctions operated at 11 GHz. A bias control circuit that achieves milliampere drive capability, transient suppression, and submicrosecond settling time is used for fast, automated measurements of A/D converter linearity, squarewave synthesis at 400 Hz, and a test for subnanovolt accuracy.

Introduction

The circuits described in this paper define a new class of Josephson voltage standard (JVS) in which the output voltage $V = Nf/K_{J\text{-}90}$ is defined by digitally programming the step number N. In a programmable JVS an array of nonhysteretic junctions is divided into a binary sequence of array segments as shown in Fig. 1. The microwave excitation for each junction is set to equalize the amplitude of the n=0 and n=1 steps as shown in the inset. Each segment of the array can be set to the n=-1, 0, or +1 step by applying a bias current (-Is, 0, +Is) at the appropriate nodes. The combined step number N for the whole array can thus be set to any value between -M and +M, where M is the total number of junctions in the array [1].

The rapid settling time and inherent step stability of the JVS in Fig. 1 make it potentially superior to a conventional JVS for dc measurements. (We define a dc measurement to be one in which the transient associated with changing N can be excluded from the measurement.) Such measurements include calibration of dc reference standards and digital voltmeters, and the characterization of A/D and D/A converters. The circuit of Fig. 1 can also be used to generate a staircase approximation to a sinewave by selecting appropriate step numbers in rapid succession. In theory, the resulting waveform has a computable rms value and might be used to confirm the ac-dc difference of a thermal voltage converter and for other ac measurements. In the case of ac measurements, however, the transient waveform during step transitions is included in the rms value and may lead to an unacceptably large uncertainty. Practical measurements may also require an output current of several milliamperes - well beyond the current sourcing capability of a typical Josephson array. These problems are resolved by the shaded portion of Fig. 1 - an addition to the bias circuit that can amplify the output current and minimize transients at the step transitions.

Bias-Circuit Design

The bias circuit of Fig. 1 has been developed for evaluating and optimizing the performance of programmable Josephson arrays with up to 24 segments. Under the control of the system computer it can individually measure the I-V curve of each array segment to confirm functionality and to select the optimum bias points for the -1 and +1 steps. With the optimum bias current values latched into the D/A converters, any specified dc value Nf/K_J is generated by setting the analog switches to bias the appropriate array segments into the +1, 0, or -1 states. To synthesize an ac waveform, the computer loads the waveform memory with the required state (-1, 0, or +1) of each array segment for up to 65 000 time steps of the specified waveform. When the waveform clock is started, the memory steps through the time sequence and its outputs drive the analog switches that select the bias appropriate to the -1, 0, or +1 steps for each array segment. The outputs of the analog switches control fast constant current drivers for the array bias lines. A latch on the digital inputs to the analog switches ensures that all switches change state simultaneously. The settling time of the bias current drivers is 400 ns.

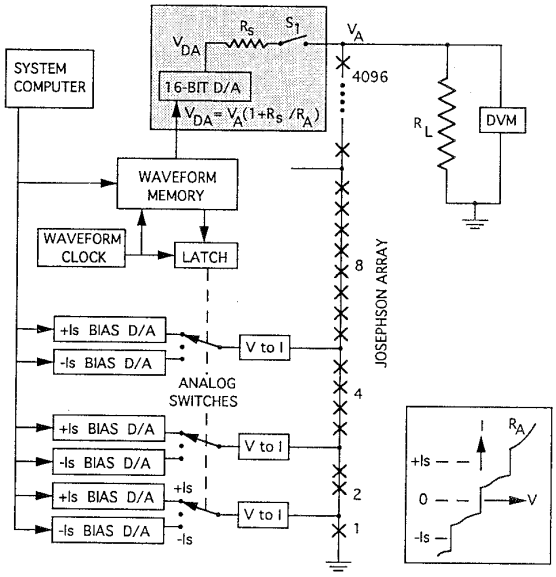

Fig. 1 A programmable Josephson voltage standard.

When switch S_1 is closed, the 16-bit D/A converter in the shaded portion of Fig. 1 can provide a substantial amplification of the available output current. This occurs because the D/A converter is programmed to provide the predicted load current and the Josephson array need only supply the difference from the predicted value. Thus, if the prediction is accurate to 1%, then the circuit can multiply the available output current by a factor of 100.

If R_s is of order 1-10 Ω, then the shaded circuit will also suppress the transients that occur when the Josephson array switches between steps. Consider the transition from N=127 to N=128. In this case six array segments with a

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total of 127 junctions will make a transition from 1 to 0 and one segment with 128 junctions will make a transition from 0 to 1. For the worst case timing error with S_1 open, the voltage during the transition could be as small as 0 or as large as 255 f/K_J. With S_1 closed, the array bias circuit can be represented by Fig. 2. Here, the array and its segment bias currents are approximated by a voltage source of value Nf/K_J in series with a resistance R_A that is shunted by switch S_A. R_A is the resistance of the array for currents outside the range of the constant voltage steps (see Fig. 1 inset). Typically $R_A = Mf/K_JI_c$ = 1 to 10 kΩ. For currents within the range of the step, switch S_A closes. During the transient S_A is open and the sensitivity of the load voltage to the array transient is given by $dV_L/dV_A = (R_sR_L) / (R_sR_L+R_AR_s+R_AR_L)$. For typical values R_A = 1 kΩ, R_L = 1 kΩ, R_s = 1 Ω, the sensitivity is dV_L/dV_A = 0.001. The transient in the array voltage is thus attenuated by a factor of 1000. As the transient dies out, I_A will fall within the step range (S_A closes) and V_L settles to exactly V_A. Thus the load voltage is controlled by the array between transitions and by the 16-bit D/A during transitions. State-of-the-art 16-bit D/A converters are capable of reducing the transient to about Φ = 60 pV· s. Assuming the worst case in which all of the transient errors add constructively, the resulting RMS error in a 1 V, 60 Hz sinewave approximation with 256 transitions would be about 1 ppm.

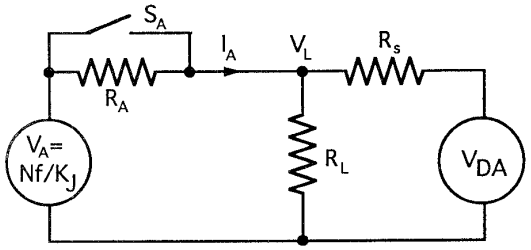

Fig. 2 An equivalent circuit for the array bias circuit.

Experimental Results

Experimental realization of the programmable JVS is being pursued with both superconductor-insulator-superconductor (SIS) and superconductor-normal-metal-superconductor (SNS) junctions. An array of 8192 shunted SIS junctions has been fabricated. It is designed to generate voltages from -1.2 to +1.2 V with 14 bits of resolution. Flaws in the largest array segments have limited its range of operation to -0.3 to 0.3 V. Using the functional 12 bits of the 8192 junction array, an accuracy test of the complete JVS system is made by switching the array from having all junctions in the 0 state, to having half the junctions in the +1 state and half in the -1 state. If the difference in array voltage between these two bias conditions remains 0 over a range of bias current, then there is very strong evidence that all junctions are generating the correct voltage. In a typical such measurement using 1024 junctions we found a difference voltage of 0.1 nV with an uncertainty of 0.3 nV (0.001 ± 0.003 ppm).

In a second fully automated experiment we used a DVM to measure the array voltage on every step from N=-750 to N=+750. Figure 3 is a plot of the linearity deviation of the DVM relative to the array for the 1500 data points.

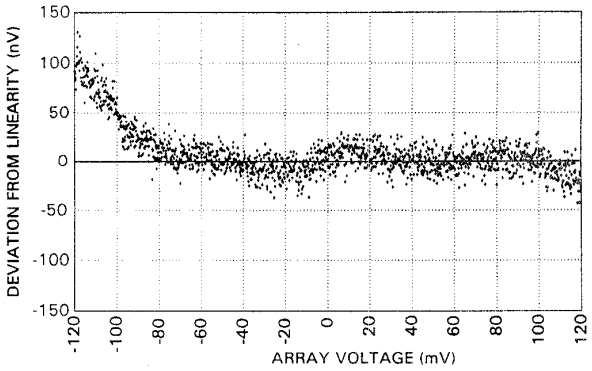

Fig. 3 Linearity deviation of a DVM as measured by an 8192 junction programmable Josephson array.

We have synthesized a 400 Hz square wave and confirmed that its RMS value remains constant over a 30 μA range of junction bias currents. This proves that all junctions are operating on constant-voltage steps and that the output voltage is therefore accurately controlled by the Josephson array. We are adding a new low loss cable to our cryoprobe. It will allow the first high accuracy measurements of the ac/dc difference of a thermal voltage converter.

SNS junctions are inherently self shunted and offer the potential for operation at much lower excitation frequency (10-20 GHz) with much larger step amplitudes (1-5 mA)[2]. Figure 4 shows I-V curves of the segments 512, 1024, 2048, 4096 and all 8192 junctions of an 8-segment SNS junction array operated at 11 GHz. (The maximum voltage is 186 mV.) The n=-1, 0, and +1 steps are all larger than 1 mA and occur over identical bias current ranges for every segment. A 32 000 SNS junction array that is designed to reach 1 V is under development.

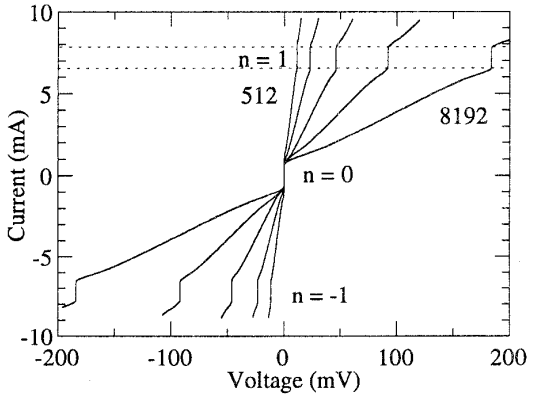

Fig. 4 I-V curves of an 8192 SNS-junction array.

[1] C. A. Hamilton, C.J. Burroughs, and R.L. Kautz, "Josephson D/A Converter with Fundamental Accuracy," IEEE Trans. Instrum. Meas, vol. 44, pp. 223-225, April 1995.

[2] S.P. Benz, "Superconductor-normal-superconductor junctions for programmable voltage standards, "Appl. Phys. Lett., vol. 76, pp. 2714-2716, Oct. 1995.