Improved Time-Base for Waveform Parameter Estimation

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Abstract

An improved gated-oscillator time-base and associated auto-calibration algorithm for use in a high-accuracy sampling waveform acquisition system are described. The time-base architecture consists of a stable 100 MHz gated-oscillator, 24-bit counter chain, and a clock period interpolator. The nominal, uncorrected linearity of the time-base is approximately ∀30 ps. By using an iterative, sine-fit based algorithm, the linearity has been improved to <∀5 ps. Details of the performance and major sources of error of the time-base and correction algorithm in an equivalent time sampling system are also discussed.

I. Introduction

Time-base performance has a significant effect on the ability of a sampling instrument to accurately measure a time-varying signal. Non-ideal time-base behavior causes deviations in the sample times that distort the sampled data. These sample time deviations have both deterministic and random components. It has been shown that, if these deviations can be measured, then either the sampled data can be corrected, or the sampling intervals can be adjusted to eliminate the distortion [1-5].

A voltmeter based on sampling principles has recently been developed at the U.S. National Institute of Standards and Technology (NIST) for making accurate rms measurements of repetitive signals ranging in frequency from 10 Hz-200 MHz [6]. The original time-base used in this voltmeter consisted of an 18-bit digital-to-analog converter (DAC) and a series of 20, successively longer, linear voltage ramps in a 1-2-5 sequence. A sampling strobe pulse was produced from the time-base by a voltage comparator at the instant the ramp voltage passed through the DAC reference voltage. While this time-base exhibited adequate performance for making rms voltage measurements, its linearity and jitter were found to be inadequate for making other time-domain measurements. For example, the measurement of repetitive, short transition-duration (<100 ps) voltage steps over a long time period (10 μs) is useful for determining the waveform parameters of step generators and the impulse response of analog-to-digital converters (ADCs) and linear networks.

An improved, gated-oscillator time-base has been designed and constructed that overcomes the limitations present in the original design. While its uncorrected performance is impressive, a new auto-calibration hardware and software scheme has been developed to further improve its timing linearity. The auto-calibration scheme employs a time-base error estimation algorithm similar to one proposed in [7], but with important additional details necessary when implementing the scheme as an embedded, steady-state, iterative process.

II. Operating principle

The function of the gated-oscillator time-base is to produce a series of strobe pulses that are coherent to a trigger signal for purposes of sampling a signal in one of two sampling modes, equivalent time or quasi-equivalent time. When used to sample a signal in equivalent time sampling mode, the time-base outputs a single strobe pulse for each trigger occurrence. When used to sample a signal in quasi-equivalent time (or Aleapfrog≅) mode, the time-base outputs multiple strobe pulses for each trigger occurrence. This mode of operation offers significant advantages in terms of acquisition speed when sampling low-frequency signals. For a detailed discussion of equivalent time vs. quasi-equivalent time sampling, see [6].

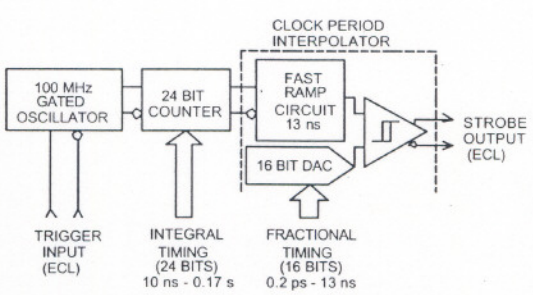

Fig. 1. Simplified diagram of the gated-oscillator time-

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base.

A simplified diagram of the gated-oscillator time-base is given in fig. 1. The time-base incorporates high speed, differential, emitter-coupled logic (ECL) and consists of a 100 MHz gated oscillator, a 24-bit programmable counter chain, a clock period interpolator, and strobe pulse output shaping and driver circuits (not shown in fig. 1). The delay from a trigger input signal can be programmed to an integral number of clock oscillator periods ranging from 10 ns to 0.167 s. The delay resolution is enhanced by a high speed vernier ramp system designed to interpolate one period of the clock pulse to a resolution of 16 bits (0.2 ps).

The time-base has a minimum trigger-to-strobe delay on the order of 25-30 ns due to inherent system delays and oscillator startup behavior. A detailed discussion of each major section of the time-base is given below.

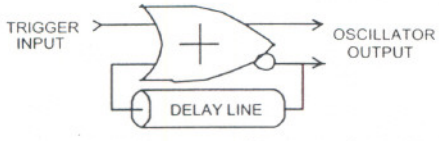

Fig. 2. Simplified diagram of the gated-oscillator.

A. Gated oscillator

A simplified diagram of the gated-oscillator is given in fig. 2. The oscillator consists of a two-input ECL logical-OR gate, a 50 ohm, coaxial transmission delay line, and output shaping and driver circuits (not shown in fig. 2). The oscillator is disabled when the trigger input is in a logic high state. When the trigger input goes low, the output of the OR gate will change state, changing its complementary output from low to high. This transition will be sensed at the OR gate=s input after propagating through the delay line, thus causing the OR gate to change state again. The circuit will oscillate with a period given by

$$T_{osc} = 2t_g + 2t_l \qquad (1)$$

where t_g is the gate propagation delay of the OR gate (approximately 300 ps), and t_l is the propagation delay of the transmission line (4.7 ns). The oscillator=s ability to maintain a steady frequency from its oscillation onset (lack of FM) is largely dependent upon the t_g term in (1). This term stays relatively constant, because once the gate reaches thermal equilibrium, the power dissipated within the chip remains essentially the same whether in standby or oscillating mode.

B. 24-bit counter

The counter in fig. 1 consists of a cascaded chain of 3, 8-bit counters (programmed via the 24-bit integral timing word). Each of the three counters is designed to count up and output a logic pulse when a terminal count is reached. To minimize the counter=s timing linearity errors, particular care was taken in the printed circuit board layout to match the line lengths and impedances of the terminal count output of each counter in the chain. The terminal count outputs of the three counters are logically ORed together and used to trigger the fast ramp circuitry of the clock period interpolator.

C. Clock period interpolator

The purpose of the clock period interpolator in fig. 1 is to increase the timing resolution of the counter from 10 ns to 0.2 ps. The interpolator consists of a 13-ns (0.25 V/ns) linear ramp generator, a 16-bit DAC, and a high speed comparator. The comparator will rapidly change state to produce a strobe pulse when the linear ramp signal crosses a pre-defined voltage level, determined by the 16-bit DAC=s fractional timing word. It is important to note that only the middle 10 ns of the 13-ns ramp is used in an acquisition; the remainder of the ramp allows for timing overlap of the gated-oscillator period. The instant the strobe pulse is generated, the ramp circuit is reset. A pulse stretching circuit (not shown in Fig. 1) maintains the strobe pulse width at a nominal 10 µs. It is during this 10 µs interval that the time-base control circuits update and load new integral and fractional timing words for the next strobe pulse to be generated.

III. Sources of error

A. Quantization errors

The timing relationship between the trigger input signal and the strobe pulse output is quantized, with a resolution determined by the counter and the 16-bit clock period interpolator. As stated in [6], this quantization causes noise in the sampled signal data that is similar to jitter, but cannot be reduced by averaging, since the noise is deterministic and correlated to the input signal. This noise will cause errors in waveform parameter estimates that are difficult to predict, although error bounds for the estimate of the rms value of a sinewave have been determined [8,9]. The approach taken in the design of this time-base has been to give the time-base adequate resolution (0.2 ps) to minimize the effects of quantization, relative to other sources of error.

B. Linearity errors

The gated-oscillator frequency settling will frequency modulate the time-base output and cause a dynamic timing linearity error. While the exact amount of modulation and its rate of decay is difficult to measure directly, it will be shown

that the time-base error estimation algorithm is sensitive to this modulation and indicates that this error component is insignificant.

Timing mismatches between the terminal count outputs of the 3, 8-bit cascaded counters that make up the 24-bit counter can affect the static timing linearity of the time-base. The effect is analogous to the way resistance mismatch can affect the static linearity of an R-2R ladder DAC. As stated earlier, the impedances and timing delays of the transmission lines carrying these signal were carefully matched to minimize these errors.

The clock period interpolator is another source of timing linearity error and is composed of four major factors: the voltage linearity error of the 16-bit fractional timing DAC, the voltage linearity error of the comparator, the voltage linearity error of the ramp, and the timing scale factor mismatch between the gated-oscillator period and the ramp slope. The overall interpolator error can be modeled as a linear combination of these four factors. These errors are measured and compensated dynamically, as described in section IV, below.

C. Jitter

The time-base jitter has been measured using a commercially-available time interval analyzer. Results indicate that the time-base exhibits less than 7 ps of jitter for trigger-to-strobe delays from 10 ns to 100 ns. For longer delays, the time interval analyzer measurements indicate that the jitter increases, leveling off to a value that is less than 1 part in 10^6 of the trigger-to-strobe delay. It is unclear whether the increased measured jitter is due to the time-base or the measurement instrument. Taking the worst-case measured jitter (7 ps) into account and calculating its effect on the expectation of the rms estimate of a 200 MHz (5 ns) sinewave, the rms value is reduced by only 40 parts in 10^6 [10]. In situations where it is necessary to compensate for jitter effects, the deconvolution methods of [11] may be used.

IV. Time-base error compensation

In addition to the basic circuitry of fig. 1, the gated-oscillator time-base design includes auxiliary hardware and software to measure the time-base errors and compensate for them in a closed-loop system. A detailed discussion of each major component of the time-base auxiliary compensation (auto-calibration) system is given below.

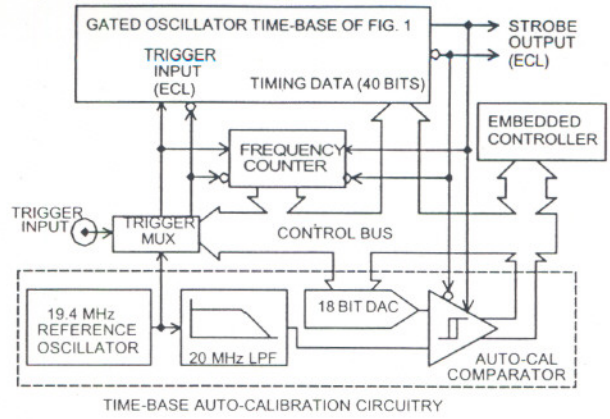

Fig.3. Simplified diagram of auto-calibration hardware.

A. Auto-calibration hardware

A simplified diagram of the time-base, including the auto-calibration hardware, is shown in fig. 3. The purpose of the auto-calibration hardware is to provide an internal, equivalent time sampling channel to the time-base. The functional blocks of this internal sampling channel are interconnected through a common control bus driven by an embedded PC controller.

In normal operating mode, the trigger multiplexer (mux) is switched so that the time-base is driven by the trigger input signal. The frequency counter, with a resolution of 5 parts in 10^7 for input frequencies from 10 Hz to 200 MHz, is then used to measure the trigger input signal frequency. The controller then calculates the optimal set of 40-bit (24 counter bits + 16 DAC bits) timing data values necessary to provide an exact integer number of strobe output pulses per period of the input trigger.

During a time-base auto-calibration sequence, the 19.4 MHz, ECL reference oscillator is used to drive both the trigger input of the time-base and the frequency counter. This oscillator's output is also converted to a low-distortion sinewave (THD < 0.1%) by the 20 MHz, 8-pole, Butterworth, low-pass filter. The embedded controller measures the sinewave signal in equivalent time using the auto-cal comparator, a high speed latched IC analog comparator of the type described in [12]. The comparator's latching inputs are driven by the time-base's strobe outputs and its reference is supplied by the 18-bit DAC. The frequency of the gated-oscillator is measured by configuring it to operate in a free-run mode. The reference oscillator frequency, the low-distortion sinewave data, and the gated-oscillator frequency are used to estimate the time-base linearity errors, using the auto-calibration software method described below.

B. Auto-calibration software

In the approach taken to correct the time-base distortion, it is assumed that the gated-oscillator exhibits insignificant levels of dynamic nonlinear behavior (time-dependent FM). The validity of this assumption will be evident from the corrected time-base measurement results. The correction algorithm attempts to correct only the gain mismatch between the gated-oscillator frequency and the ramp slope, and the nonlinear behavior of the ramp. The basic steps that are performed by the time-base correction algorithm are as follows:

1. Initialize a 128-point time-base correction array to zero.
2. Calculate the 512-point, 40-bit timing data array for the time-base, based upon the measured 19.4 MHz reference frequency. Correct the 16-bit fractional timing DAC settings portion of the data using the 128-point time-base correction array. Use linear interpolation between the correction data points to determine the correction for each fractional timing DAC value.
3. Perform an equivalent time sampling acquisition of the filtered reference oscillator signal using the corrected 512-point timing data vector. Estimate the time-base distortion using the acquired sinewave data, the measured 19.4 MHz reference frequency, and the measured gated-oscillator frequency.
4. Reduce the 512-point distortion estimate to 128-points using block-averaging and IIR filtering.
5. Update the time-base correction array by adding to it the 128-point distortion estimate, calculated in step 4.
6. Return to step 2.

In step 3, The time-base distortion is extracted from the 19.4 MHz low-distortion sinewave data using the constant-waveshape constraint, iterated sine-fit method, described in [7]. It is beyond the scope of this paper to provide an in-depth discussion of this method, other than to note that only the fundamental harmonic is considered in the fit, and uniform weighting is used in the time-base distortion estimate. However, the auto-calibration circuitry provides no means of sampling the 19.4 MHz signal over multiple phases directly, as is required in [7].

The fit returns a 512-point, time-base distortion estimate array that contains approximately 10 repetitions of the ramp errors. Since each sample in the sinewave data corresponds to a known 40-bit timing data value, the time-base distortion estimate array elements are then sorted according to the corresponding 16-bit fractional timing word used to acquire each element. The resulting 512-point array contains an estimate of the nonlinearity of a single ramp. The 512-point array is then reduced to 128 points by block-averaging the data. The blocks are chosen by segmenting the 2^{16} possible fractional timing DAC values into 128 groups. Since only the middle 10 ns of the 13-ns ramp is ever used, this results in an array with many undefined values at the beginning and end; these values are set to equal the nearest defined value.

The 128-point time-base distortion estimate is used as an integrated feedback constant in the calculation of the 128-point time-base correction array. This can lead to instability of the time-base correction algorithm, since adjacent members of the distortion estimate array may be weakly and/or unevenly correlated. To increase feedback stability, the distortion estimate array is time-reversed and filtered using a causal, 4-pole, low-pass, Bessel, IIR digital filter. The filtered data is then time-reversed again and filtered a second time. Applying the IIR filter in this way tends to cancel the filter's phase delay. The filter's corner frequency is chosen so that the filter settles well before processing the active region (defined values) of the distortion estimate array.

V. Test results

Figures 4 and 5 show the estimated linearity of the new time-base at the start of the auto-calibration algorithm, and after several iterations, respectively. The discrete data points

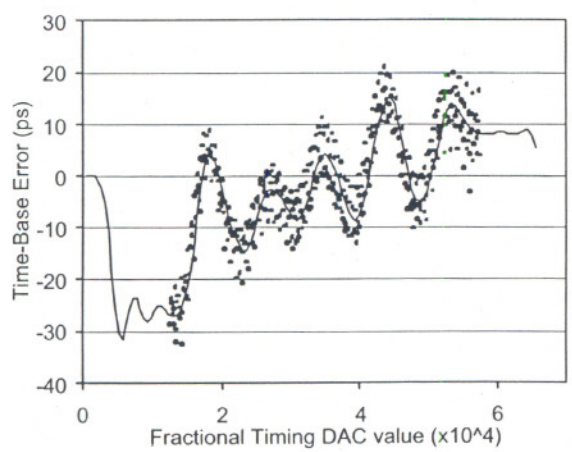

Fig. 4. Uncorrected time-base errors.

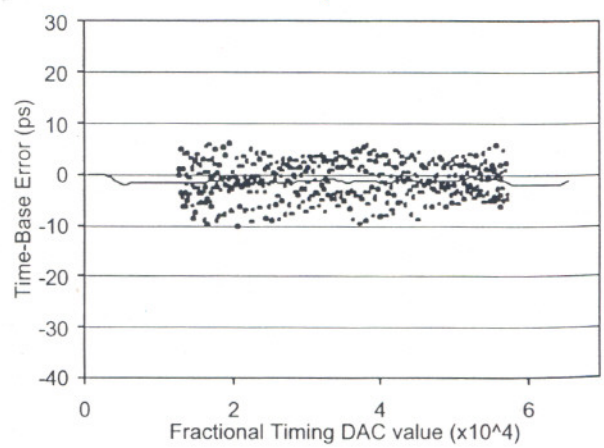

Fig. 5. Corrected time-base errors.

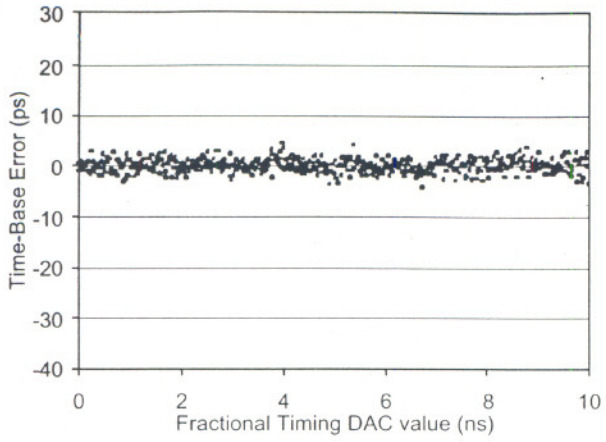

Fig. 6. Time-base errors using methods in [7].

in the plots represent the raw, unfiltered output of the sine-fit distortion estimate algorithm. The solid lines in the plots represent the same data, after applying the IIR filtering.

It is important to note from these plots that the discrete points represent timing errors extracted from several consecutive fractional timing ramps, sorted into a single ramp. The fact that they overlie one another very closely tends to validate the assumption that the gated-oscillator exhibits very little FM modulation during startup.

To check the performance of the auto-calibration algorithm, the corrected time-base was used in a waveform acquisition system, described in [6], to acquire 4 records of sinewave data at 2 different phases and frequencies. The data was then processed to extract the time-base linearity errors using the techniques described in [7]. The results are shown in fig. 6 and indicate an rms error of approximately 1.4 ps. The reduced variance of the fig. 6 data relative to figures 4 and 5 is due to two factors: increased sample averaging was used to acquire the sinewave data for fig. 6, and the error estimation algorithm used for fig. 6 more accurately rejects the distortion due to the sampling channel. Much of the apparent noise in figures 4 and 5 is due to residual sampling channel distortion that has not been rejected by the auto-calibration algorithm.

VI. Conclusions

An improved time-base and auto-calibration system for use in a high-accuracy, equivalent time waveform acquisition system has been described. The time-base error estimation algorithm has been shown to provide very good performance when used in a closed-loop system. The overall performance of the time-base when used in a waveform acquisition system was verified using techniques that more accurately take into account the signal distortion caused by the sampling channel, as discussed in [7].

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