USE OF THE OSCILLATION BASED BUILT-IN SELF-TEST METHOD FOR SMART SENSOR DEVICES

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ABSTRACT

An oscillation-based built-in self-test (BIST) method is presented for functional testing of mixed signal devices. An integral component of this method of on-chip testing involves transforming a static analog signal into a digital clock-like signal. This paper focuses on comparing the results of various analog-to-digital converters (ADCs) used to evaluate the functional integrity of a biosensor. The objective of this research is to determine key metrology infrastructure issues needed for developing the design reuse approach for multi-technology System-on-a-Chip (SoC) devices.

1. INTRODUCTION

The driving force in today's semiconductor industry is the need to maintain a rate of improvement in speed and size reduction of 2x every eighteen months in high-performance components. Currently, these improvements rely exclusively on advances made in semiconductor miniaturization technology. The 1999 ITRS (International Technology Roadmap for Semiconductors) suggests that, "innovation in the techniques used in circuit and system design will be essential to maintain the historical trends in performance improvement" [1]. Achievement of this advancement in circuit and system design techniques is increasingly becoming dependent on integrating multiple silicon technologies on the same chip. The devices that result from these integrations are commonly referred to as System-on-a-Chip (SoC) devices.

Design is paramount for all categories of the ITRS roadmap. This is especially true for the SoC category where time-to-market for an Application Specific Integrated Circuit (ASIC) is a key attribute for new product delivery. Design is additionally important for SoC devices because of increasing system complexity. The growth of system complexity is due to the diversity of SoC design styles, integrated passive components, and the increased need to incorporate embedded software. Design for SoC devices will become increasingly difficult with the growing interaction among design levels, the difficulties of converging multiple designs onto a single chip, design process predictability, and the growing size and dispersion of design teams.

These challenges are overcome with the use of block-based design approaches that emphasize design reuse. System blocks often contain a layout file that is used for the fabrication process and an Analog Hardware Description Language (AHDL) behavioral model used to describe the interaction of system components during the design process. Each system block should have features that allow for the implementation of Built-in Self-Test (BIST). The emergence of the SoC paradigm imposes various metrology and standardization challenges. These include metrology for multi-technology process monitoring, BIST calibrations, validation of behavioral model representations, and benchmarking simulation of on-chip systems interactions.

Another significant challenge involves ensuring the testability of an IC design. This is a formidable task, as testability within the context of mixed technology integrated circuits is not well defined. Testability is defined as controllability and observability of significant waveforms within a circuit [4]. For most IC designers, significant waveforms are input/output signals that can be obtained at every stage of the circuit. The first stage of the circuit input is assumed to be controllable; while during the last stage, output is observable.

Some have proposed methods of assuring testability that involve the use of oscillatory BIST techniques [5,6]. The BIST method using an oscillation-based test circuit has been shown to have the potential of overcoming common problems associated with conventional test methods [6]. This BIST method has also been shown to be effective for any type of mixed analog/digital circuitry used as system blocks [7].

In this paper, the Analog to Digital Converter (ADC), a key component of BIST circuitry capable of interfacing with mixed-signal devices, is analyzed. Specifically, the focus is on the use of oscillation-based digital circuits for mixed signal testing including the production line technique of using standard ring oscillator properties. It is expected that this work will lead to establishing the test metrology necessary for developing BIST methods that incorporate the use of analog-to-digital system blocks.

2. BUILT-IN SELF-TEST

Involved in testing an IC are the direct costs associated with procurement of test equipment and time to test and the indirect costs of developing test procedures. Moreover, the analog portion of mixed analog/digital circuitry, although typically making up less than 10% of the overall chip area, requires test procedures that tend to dominate the test time of mixed technology chips. This is due to the following:

- Accurate analog signal sources must be applied to the Circuit Under Test (CUT).
- Specialized equipment containing precision circuitry must be used to test Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs).
- Package and test system interconnects that connect the CUT to the ADCs and DACs of the tester often introduce parasitics that affect the performance of the chip [3].

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BIST methods are expected to assist designers in avoiding many of these concerns.

In general, BIST circuitry is made up of the following three key components: a controller, a pattern generator, and a multiple input signature analyzer [3]. The BIST method allows system block testing to be realized by commanding the core BIST controller to initiate self-test and by then comparing the output to the known correct result. On-chip testing of embedded memories can be realized by either multiplexing their address and data lines to external SoC I/O pads or by using the core processor to apply enough read/write patterns of various types to insure the integrity of the memory. Another approach is to provide embedded memories with their own BIST circuitry [8].

To be effective for SoC devices, the BIST approach must provide a means for on-chip test response measurement, on-chip test control for digital and analog test, and I/O isolation. There are three categories of measurements that can be distinguished: static, small signal, and time domain. The static tests include the determination of the steady-state operating points, offset voltages, bias voltages, and circuit gain. Static faults can be detected by a single set of steady-state inputs. Small signal dynamic tests measure the frequency response of the system under test. The input stimulus is usually a sinusoidal waveform with variable frequency. Digital Signal Processing (DSP) techniques can be employed to perform harmonic spectral analysis. Time domain measurements derive slew rate and rise and delay times using pulsed signals, ramps, or triangular waveforms as the input stimuli of the circuit.

A multi-function smart biosensor circuit is analyzed in this paper to provide an example of the expected results that are possible when using various ADCs to verify the structural and functional integrity of the CUT.

3. BIOSENSOR CIRCUIT DESCRIPTION

A multi-function smart sensor system can be used to identify the properties of a fluid. This technology is of interest to a number of areas including: ecology, food processing, and health care. In biomedical engineering, biosensors are becoming of considerable importance. In this area biosensors can be used in clinical analyses for the selective determination of properties of fluids including blood, urine, and saliva.

The class of biosensors studied in this work is designed to analyze physical properties of fluids [13]. These sensors are capable of deciphering various characteristics associated with fluids including: color, odor, pH, resistivity, and dielectric constant. The sensors can also discern inorganic and organic chemical properties. Such sensors are implemented using micro-electro-mechanical systems (MEMS) technology. The sensor circuit can be fabricated on a semiconductor substrate that allows for the integration of additional signal processing circuitry onto the chip. An array of such sensors can be used to determine multiple properties of a fluid, using a single chip.

Figure 1 is a schematic of the type of sensor used to detect fluid properties. This example sensor circuit operates as a dielectric constant measurement device. This sensor can be provided as part of an integrated micro-system designed to determine the properties

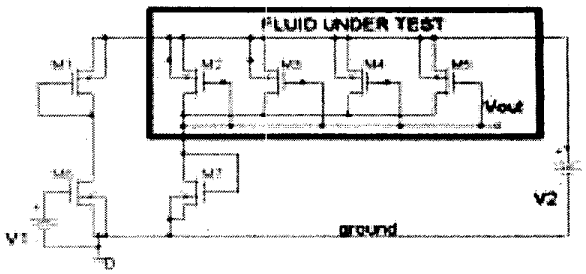

Figure 1. Schematic of biosensor circuit under test. Each transistor has a W/L ratio of 10μ/10μ. The overall W/L ratio of the fluid-sensing transistor is therefore 40μ/40μ.The output of this circuit is taken as the gate of transistor M5.

of a fluid. The fluid-sensing transistor in this sensor is a VLSI adaptation of the CHEMFET [9]. The sensor operates as a capacitive-type bridge such that a balance can be set for a normal dielectric constant. In the presence of a fluid, the unbalance that occurs within this sensor bridge is used to evaluate the fluid's dielectric constant. The four CMOS transistors form the bridge: M1, M6, M7, and the fluid-sensing transistor comprised of transistors M2 through M5. The fluid-sensing transistor and transistor M1 are PMOS (p-type MOSFETs) transistors in the diode connected configuration (gate connected to drain) while the lower two, M6 and M7, are NMOS type (one diode connected and the other with a gate voltage control). The output, Vout, of the sensor circuit is taken between the junction of the fluid-sensing transistor and the diode connected transistor, M7.

The transistors, M2 through M5, have openings in their gates to allow fluid to flow between the silicon substrate and the polysilicon gate where the gate oxide has been removed. This allows the fluid to behave as the gate dielectric for that transistor. The fluid-sensing transistor is constructed out of four transistors with all terminals connected in parallel to increase the gain constant parameter KP that is proportional to the dielectric constant.

Fabrication of the sensor is based on a sacrificial etch process, where the silicon dioxide gate dielectric in the fluid-sensing transistor is removed by chemical etch [12]. This activity is accomplished by opening holes in protective layers using the over-glass cut method available in the MOSIS-MEMS fabrication process.

A critical step in providing a BIST methodology for this circuit or any analog circuit involves converting the CUT's static analog output signal into a digital signal using an ADC. A specialized oscillation-based ADC conversion is further discussed in the following section.

4. OSCILLATION-BASED BIST

Converting the output of the analog CUT into a digital signal involves transferring the signal through an ADC comprised of a Voltage Controlled Oscillator (VCO), Level Crossing Detector (LCD), and Frequency Counter (FC). The LCD and FC make up the frequency-to-number converter (FNC) which passes a number to a frequency counter for processing. A block diagram of this

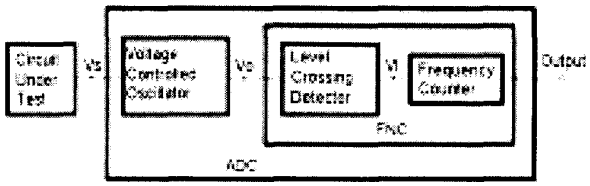

Figure 2. Block Diagram of ADC Conversion Process.

ADC conversion process is shown in figure 2. The frequency counter output that appears at the output of this diagram can be expressed as a function of the CUT's components or parameters [7]. Changes in various component characteristics (i.e., transistor W/L ratios) will give rise to deviations in the CUT's expected output. The test for a fault is therefore denoted by any deviation of an oscillation frequency from its expected nominal value.

The question then arises as to how to transform the CUT signal to an oscillating signal. For the case of a steady-state voltage output, oscillations are created with the aide of a voltage-controlled ring oscillator. An example of a VCO is provided in figure 3.

The VCO is a structure made up of three unique parts including: the control input stage, the propagation delay controlled ring oscillator, and the output buffer. The input control voltage (Vin) that originates from the circuit under test controls the overall oscillation frequency of the VCO. This voltage is capable of "current starving" the inverter stages of the ring oscillator and thus changing the propagation delay. The input sets the current in the current sources M5 and M20 of figure 3, which in turn set the current in the delay control elements. The ON resistance of the pull-up (upper transistors of ring oscillator) and pull-down (lower transistors of ring oscillator) transistors is modulated according to the input voltage, Vin. These variable resistances control the current available to charge and discharge the load capacitance of each inverter stage in the ring oscillator. When the control voltage is large, a large current will flow, producing a small resistance and thus a small propagation delay.

Each of the inverters appearing in the VCO ring oscillator consists of two complimentary transistors (an NMOS and a PMOS). A ring oscillator consists of an odd number of inverters. The output of the last inverter is connected to the input of the first. The minimum number of inverters needed to produce oscillations is three. The oscillation frequency (f_{osc}) is inversely proportional to the gate propagated delay time and the number of gates n, $f_{osc}= 1/(2n\tau_{osc})$.

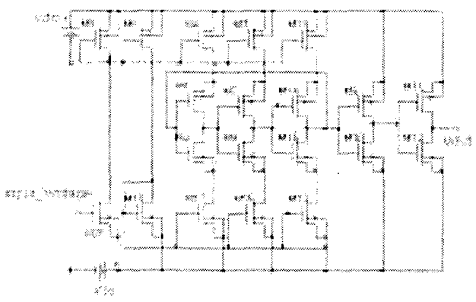

Figure 3. Voltage Controlled Oscillator. This VCO is made up of an input buffer, propagation delay controlled 3-stage ring oscillator, and an output buffer. Each transistor shown has a W/L ratio of 10µ/10µ.

In this analysis, various VCO configurations were considered. The key variables in the design study were those that affected the ring oscillator stage. A number of inverters and drain voltages were considered prior to selecting the configuration for the BIST method studied here. The 9-inverter ring oscillator with a drain (source) voltage of 0.25V (-0.25V) was chosen as most suitable for the BIST ADC.

The output of the VCO is fed into the input of various level crossing detectors (LCDs). Three types of LCDs are studied. The first LCD considered is a zero-crossing detector (ZCD); the second is an LCD proposed by Arabi (aLCD) [11]; while the third is referred to as the enhanced level-crossing detector (eLCD). The authors created the design for the eLCD. It is shown in figure 4 and is a two-stage device made up of a differential pair in the first stage and the aLCD in the second stage. The differential pair is attached to the input of the aLCD and serves three purposes: it amplifies the oscillating signal derived from the VCO, it provides noise immunity, and it adds a negative bias to the overall input of the aLCD. The results of the Arabi-level crossing detector, zero crossing detector, and enhanced-level crossing detector analyses are provided in the section below.

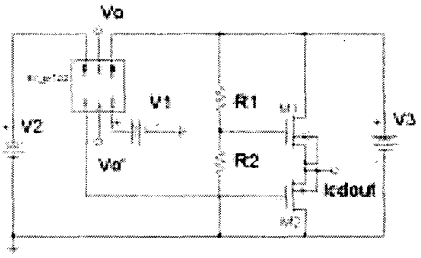

Figure 4. Enhanced Level-Crossing Detector (eLCD).

5. SIMULATION ANALYSIS AND RESULTS

Testing the effectiveness of the proposed oscillation-based BIST method involved studying the outputs of each of the stages of the ADC conversion process. The stages of interest are: the input stage (Vs), voltage-controlled oscillator output stage (Vo), and level-crossing detector output stage (Vl) as shown in figure 2.

The oscillation-based BIST method begins by stimulating the biosensor with a static input voltage of 0.5 V (V1 of figure 1). The sensor's resulting static output voltage, Vs, is then fed into the input of the voltage-controlled oscillator. The VCO transfers this static input into an oscillating voltage signal, Vo. The oscillating signal, Vo, is then passed to the level-crossing detector to obtain the output signal, Vl. Figure 5 shows examples of the signals obtained at the output of three different LCDs. Each of these signals will from this point forward be considered to be the nominal outputs for the circuit under test.

Two structural tests were performed. The first test involved removing one of the transistors from the sensor circuit and replacing it with a short circuit. This type of error could occur in practical applications as a result of a transistor that has been

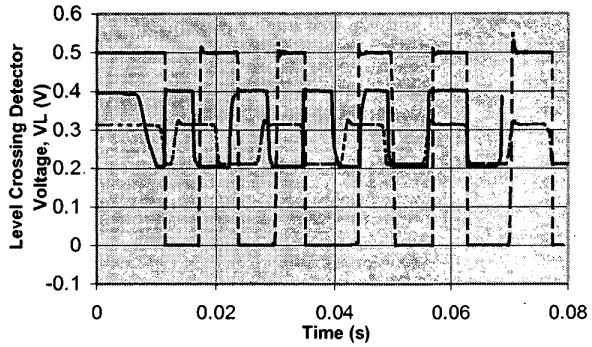

Figure 5. Plot of nominal output with enhanced Level-Crossing Detector (dashed line), Arabi Level-Crossing Detector (solid line), and Zero-Crossing Detector (small dashed line).

shorted due to incomplete etch during the MEMS fabrication process. For this test, the upper left diode-connected PMOS transistor of the fluid-sensing transistor (figure 1, see Fluid Under Test) was removed and replaced with a short circuit.

The differences from the nominal waveforms for the LCDs are shown in Figure 6. If there is no change in frequency, the signal difference will be a constant value of zero. The pulses that appear on the graph indicate the time intervals where the signal deviates from the nominal value. The plot of the enhanced LCD output difference for this functional test shows a shift in frequency. This shift would result in a frequency counter output that deviated from nominal thereby triggering an error for the

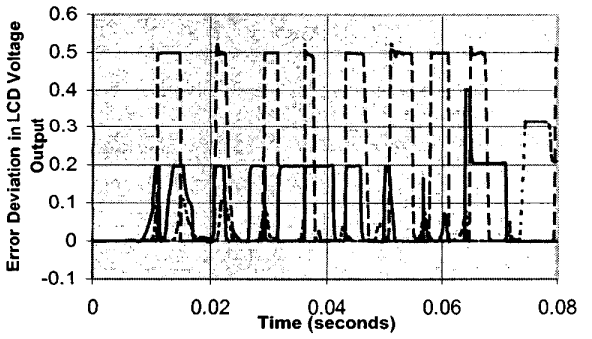

Figure 6. Difference comparison of results for functional test 1. Enhanced Level-Crossing Detector (dashed line), Arabi Level-Crossing Detector (solid line), and Zero-Crossing Detector (small dashed line).

overall oscillation-based BIST method. Similar frequency shifts are noted for the aLCD and ZCD methods although they do not appear to be as significant as the shifts obtained from the enhanced level-crossing detector.

A second functional test was performed that involved decreasing the size of the fluid-sensing transistor. This was achieved by changing the W/L ratio of transistor M2 in figure 1 from 10μ/10μ to 5μ/10μ. This test emulates a fault that could arise during the MEMS fabrication process. As expected, the outputs of the Arabi level-crossing detector, enhanced level-crossing detector, and zero-crossing detector oscillate. The ZCD method failed, however, to produce significant deviations in oscillation frequency during this functional error test. Also, while the aLCD produced oscillations that deviated from the nominal oscillations, the enhanced LCD was more effective in discerning this type of functional error. This is largely due to the differential pair that appears in the first stage of this circuit.

The differential pair amplifies the signal, Vo (figure 2), and adds a negative bias. This allows the second stage of the eLCD to truncate all negative voltage values thus producing an effective level crossing detector. In its natural state, the level crossing detector designed by Arabi appears to operate as a level shifter and signal scaler. This is shown in figure 5.

6. CONCLUSIONS

A novel BIST approach based on the oscillation-based analog-to-digital converter has been introduced. The purpose of the oscillator-based BIST method is to convert an analog output signal into a digital output that can be read by a digital counter. When applying this method to a sensor circuit, the aLCD, eLCD, and ZCD produce expected deviations in output frequency for different functional differences. An enhanced level-crossing detector is developed that improves the detection of frequency differences for sensor fault conditions. PSPICE simulations indicate that this enhanced LCD is capable of distinguishing the VCO oscillation frequency for a wide range of static input voltages. Future applications of this BIST method will use digital counters to quantify the fault conditions.

7. ACKNOWLEDGEMENTS

The authors would like to sincerely thank Muhammad Y. Afridi and Michael Gaitan for discussions that aided in producing the manuscript.

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