Electro-thermal Simulation of an IGBT PWM Inverter†

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Abstract—**A recently developed electro-thermal network simulation methodology is used to analyze the behavior of a full-bridge, pulse-width-modulated, voltage-source inverter which uses IGBTs as the switching devices. The electro-thermal simulations are performed using the Saber circuit simulator and include the control logic circuitry, the IGBT gate drivers, the physics-based IGBT electro-thermal model, and the thermal network component models for the power device silicon chips, packages, and heat sinks. It is shown that the thermal response of the silicon chip determines the IGBT temperature rise during the device switching cycle. The thermal response of the device TO247 package and silicon chip determines the device temperature rise during a single phase of the 60-Hz sinusoidal output. Also, the thermal response of the heat sink determines the device temperature rise during the system start-up and after load impedance changes. It is also shown that the full electro-thermal analysis is required to accurately describe the power losses and circuit efficiency.**

I. Introduction

Due to the increasing current density and higher power requirements of advanced power semiconductor devices such as the IGBT (Insulated Gate Bipolar Transistor), the devices dissipate a considerable amount of heat. Regardless of the electrical quality of the power semiconductor devices, the devices will fail if the heat cannot be removed effectively. In addition, the electrical performance of the system can be limited by device heating and thermal coupling between devices. Therefore, concurrent simulation of the electrical and thermal aspects of power electronic systems is essential for effective computer-aided-design (CAD) of these systems. The electro-thermal simulations also enable the design of the thermal management systems (typically one of the most costly aspects of the overall system design) to be incorporated into the original design of the electronic system.

Typical power electronic system design considerations include control system analysis, gate level logic simulation, the interaction of power semiconductor devices and magnetic components with the external circuit, and the thermal management of the power dissipated in the semiconductor devices. However, traditional circuit simulation programs such as SPICE (Simulation Program with Integrated Circuit Emphasis) [1] were developed for integrated circuit analysis and do not provide the capability to effectively analyze many of these aspects of power electronic systems. As a result, various simulation tools have been developed that specialize in the analysis of specific aspects of advanced electronic systems, such as power system simulation [2], thermal network analysis [3], and physics-based semiconductor [4] and magnetic component simulation. However, these separate tools require the designer to use different simulation environments, and only permit limited interaction between the various aspects of the overall system design.

Recent advancements in the capabilities of circuit simulation programs such as Saber™ have resulted in the capability to simulate the entire power electronic system in a single simulation environment [5]. The purpose of this paper is to apply the recently developed simulation capabilities toward the electro-thermal analysis of a full-bridge, voltage-source, pulse-width-modulated (PWM) inverter including the interaction of the different system design aspects. The abilities to accurately and effectively simulate power electronic control systems, gate level logic circuits, power semiconductor devices [6], and custom magnetic components in advanced circuit simulation programs such as Saber have been previously demonstrated. It is shown in this paper that the thermal management considerations can also be readily incorporated into the overall design process for the PWM inverter. Simulation techniques are also demonstrated that enable the designer to effectively utilize the integrated simulation capabilities and to examine the interaction between the different aspects of the overall system design.

II. Electro-thermal Network Simulation

Although SPICE-based circuit simulators [1] have traditionally been used to simulate electronic circuits using detailed physics-based semiconductor device models, these simulators do not have the capability to simulate the behavior of modern semiconductor devices which dissipate a

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considerable amount of heat. In the traditional approach used by the SPICE-based simulators, the temperature used by the device models is chosen by the user prior to simulation and remains constant during the simulation. This traditional approach is not applicable to modern power electronic devices and other advanced semiconductor devices because the new device types dissipate a considerable amount of power which increases the internal temperature of the semiconductor devices (self-heating) and increases the temperature of other adjacent semiconductor devices (thermal coupling). The unique approach taken in the electro-thermal network simulation methodology used in this paper [7] is to define the temperatures at various positions within the silicon chips, packages, and heat sinks (thermal network) as simulator system variables so that the dynamic temperature distribution within the thermal network is solved for by the simulator in the same way in which the node voltages are solved for within the electrical network.

A. Electro-thermal Simulation Methodology

Figure 1 is a diagram of the electro-thermal network simulation methodology indicating that the electrical and thermal networks are coupled through the electro-thermal models for the semiconductor devices. The electro-thermal models for the semiconductor devices (e.g., IGBTs and power diodes in Fig. 1) have electrical terminals that are connected to the electrical network and a thermal terminal that is connected to the thermal network. The thermal network is represented as an interconnection of thermal components so that the system designer can readily interchange different thermal components and examine different configurations of the thermal network. The thermal network models for power modules and heat sinks contain multiple terminals and account for the thermal coupling between the adjacent semiconductor devices.

As an example, Fig. 2a is a schematic of an electro-thermal network, and Fig. 2b is the corresponding Saber simulator netlist using the IGBT electro-thermal model [8] and the thermal component models for the silicon chip, the TO247 package, and the TTC1406 heat sink [9]. The first column of the Saber netlist in Fig. 2b specifies the name of the template that contains the model equations for each component (left-hand side of the period) and the instance within the circuit (right-hand side of the period). The remaining columns on the left-hand side of the equal signs indicate the terminal connection points of the components within the network, where the electro-thermal IGBT model is connected to both the electrical and thermal networks. The parameters used by the model templates to describe the specific components are listed on the right-hand side of the equal sign. For example, the chip area, chip thickness, and chip location on the package are changed from their default values. It is evident from Fig. 2 that the thermal network component models are interconnected to form the thermal network in the same way as the electrical components are interconnected to form the electrical network.

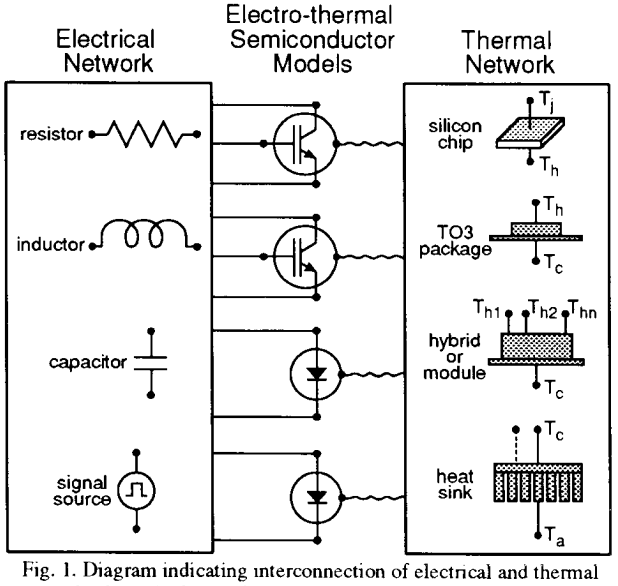
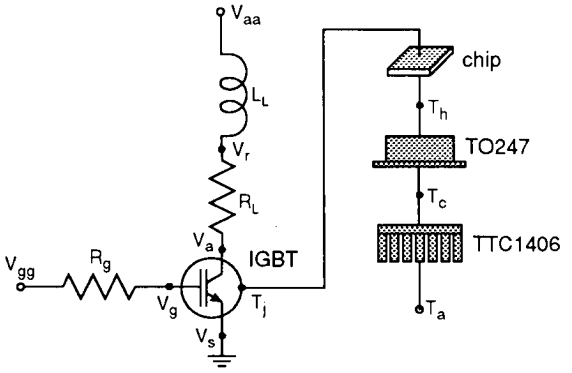


Fig. 1. Diagram indicating interconnection of electrical and thermal networks through electro-thermal models for semiconductor devices.

B. Electro-thermal Semiconductor Models

Figure 3 is a diagram of the structure of the electro-thermal semiconductor device models indicating the interaction with the thermal and electrical networks through



a)

```
#IGBT electro-thermal simulation

#Electronic network components
v.vaa          vaa  0   =   300
l.ll           vaa  vr  =   80u
r.rl           vr   va  =   30
r.rg           vgg  vg  =   10
pulsgen.1      vgg  0   =   20

#IGBT electro-thermal model
igbt_therm.1   va   vg  0   tj   = tauhl_1=1.6, kp_1=1.5

#Thermal network components
chip_therm.1   tj   th  =   thick=0.05, a_chip=0.1
to247_therm.1  th   tc  =   a_chip=0.1, ychedm=0.2
ttc1406_therm.1 tc  ta  =   a_heat=0.4
t.ta           ta   0   =   300
```

b)

Fig. 2. Example electro-thermal network a) schematic and b) netlist for an IGBT with a TO247 package and TTC1406 heat sink.

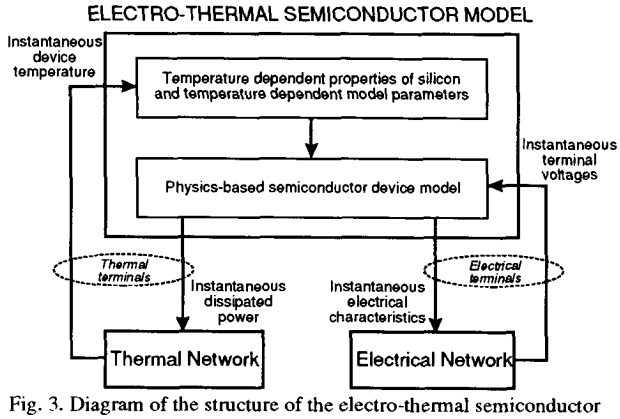


Fig. 3. Diagram of the structure of the electro-thermal semiconductor device models.

the electrical and thermal terminals, respectively [7]. The electro-thermal semiconductor models use the instantaneous device temperature (temperature at the silicon chip surface T_j) to evaluate the temperature-dependent properties of silicon and the temperature-dependent model parameters. These temperature-dependent values are then used by the physics-based semiconductor device model to describe the instantaneous electrical characteristics and the instantaneous dissipated power. The dissipated power is calculated from the internal components of current, because a portion of the electrical power delivered to the device terminals is dissipative and the remainder charges the internal capacitances. The dissipated power calculated by the electrical model supplies heat to the surface of the silicon chip thermal model through the thermal terminal.

The temperature-dependent expressions for the physical properties of silicon and the expressions for the temperature-dependent model parameters indicated in Fig. 3 are defined in [8] for the IGBT model. The temperature dependent properties of silicon are well known, and the temperature-dependent model parameters are obtained by using the extracted values of the model parameters versus temperature. An accurate extraction sequence [4] is required to resolve the temperature dependence of the model parameters. The advantage of using a physics-based model for the semiconductor devices is that the well-known temperature-dependent properties of silicon can be used to describe the temperature dependence of the model, and only a few temperature-dependent model parameter expressions must be developed. Conversely, semiconductor models that rely heavily on empirical-based formulas require calibration of each of the empirical formulae versus temperature.

The electro-thermal semiconductor models are implemented into the Saber circuit simulator by expressing the components of current flow between the electrical nodes and the components of power flow into thermal nodes in terms of the simulator system variables [8]. Simulator system variables are the voltages across the electrical nodes, the temperatures across the thermal nodes, and additional system variables that are defined to solve implicit model equations. The simulator solves the system of electro-thermal equations by iterating the system variables until the components of currents into each electrical node sum to zero (Kirchhoff's current law) and the components of power flow into each thermal node sum to zero (energy conservation). In the electro-thermal semiconductor models, temperature is a system variable that is solved for by the simulator, as opposed to traditional circuit simulator semiconductor models in which temperature is a constant parameter specified by the user. Therefore, partial derivatives of the semiconductor model equations with respect to temperature would be required to implement electro-thermal effects into SPICE-based simulators, whereas the temperature effects are implemented into the Saber simulator by simply evaluating the temperature-dependent model equations in the Saber model template [5].

C. Thermal Network Component Models

In the new electro-thermal network simulation methodology [7], the thermal network is represented as an interconnection of thermal component models where each component represents an individual building block used by the designer to form the thermal network (see Fig. 1). To use the thermal component models, the designer only needs to specify the connection points of the thermal terminals within the thermal network. The thermal models are parameterized in terms of structural and material parameters so that the details of the heat transport physics are transparent to the user. However, the user can also specify the values of the structural and material parameters in the netlist to provide accurate simulations for specific user-defined thermal component types.

Figure 4 is a diagram of the structure of the thermal component models, indicating that the thermal component models interact with the external thermal network through thermal terminals $T_1, T_2, ..., T_n$. The terminals of the thermal components can be connected to the thermal terminals of other thermal component models, to the thermal terminals of electro-thermal models, or to thermal element models such as temperature sources. The user-defined structural and material parameters (or parameters of precharacterized component library models) are used by the model to

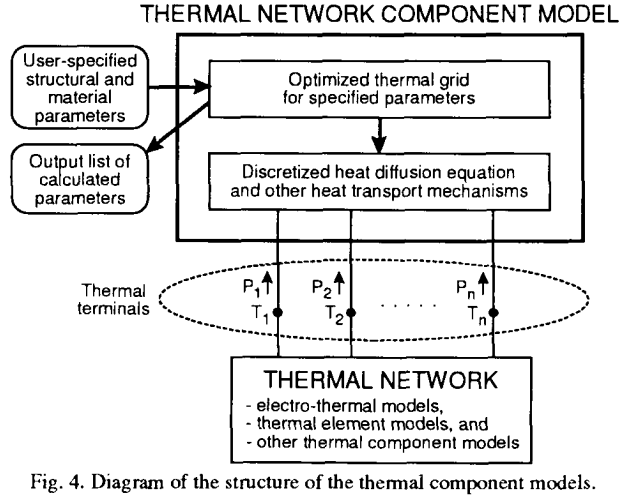


Fig. 4. Diagram of the structure of the thermal component models.

determine the heat diffusion equation discretization coefficients [9]. The thermal models also provide an output list of internally calculated parameters such as the thermal node positions that are useful for interpreting the simulated temperature waveforms.

The thermal component models are based upon a discretization of the heat diffusion equation for various three-dimensional coordinate system symmetry conditions and include the nonlinear thermal conductivity of silicon and the nonlinear convection heat transfer at the heat sink fins [9]. Because the time constants for heat flow within the silicon chip, package, and heat sink are many orders of magnitude longer than the time constants of the electronic devices and circuits, the self-heating effects behave dynamically even for circuit conditions that are considered to be steady-state for the electronic devices. In addition, for circuit conditions that result in high power dissipation levels, the heat is applied rapidly to the chip and only diffuses a few micrometers into the chip surface. Therefore, the chip-heating process is non-quasi-static, and the temperature distribution within the thermal network depends upon the rate at which the heat is dissipated. In the thermal component models, a grid spacing that increases logarithmically with distance from the heat source is used to minimize the number of nodes required to accurately represent the non-quasi-static temperature distribution for the full range of applicable power dissipation levels.

III. Electro-Thermal Network for PWM Inverter

Pulse-width-modulated voltage-source inverters are used extensively in power conversion, power conditioning, and motion control [10] due to their high energy efficiencies. The design of a PWM inverter involves the analysis of the inverter topology, the control system, the logic circuits, the interaction of semiconductor devices with other circuit elements, the analysis of motors and other load devices, and the design of the thermal management system. Until recently, the effective design of such an integrated system has been hindered by the lack of availability of simulation tools that integrate all of these aspects of the overall system design. In this section, modeling options, some recently developed, are described that enable the full integration of the overall analysis of a power electronic system such as an inverter. The procedure used to generate different inverter system topologies is also described so that the analysis presented in this work can be readily adapted to any of the many inverter topologies of interest to power system designers.

A. Circuit Topology

The basic electro-thermal network used for the PWM inverter simulations in this paper is shown in Fig. 5. Although many variations of this basic inverter are used in practice, the analysis described below using the network in Fig. 5 is representative of the type of system analysis that is applicable to all inverter circuits.

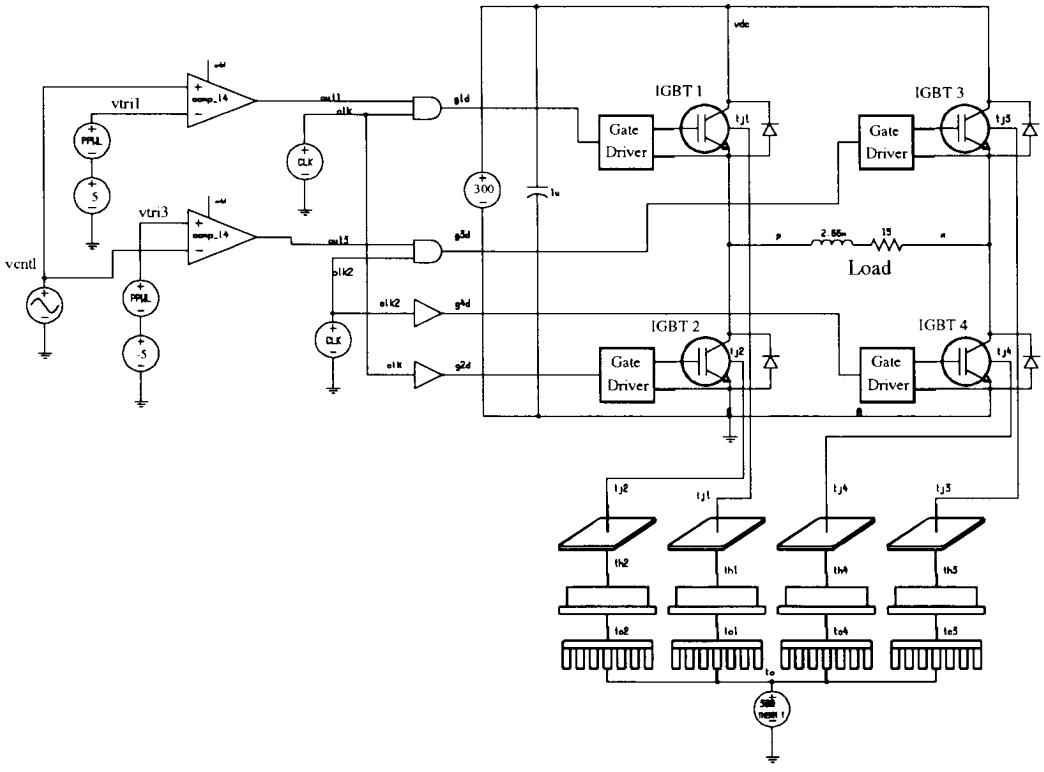


Fig. 5. The basic electro-thermal network used for the PWM inverter simulations.

In addition, a variety of modeling options may be used to emphasize the analysis of different aspects of the system design. However, the electro-thermal PWM inverter network of Fig. 5 can be readily modified as described below to represent the particular topology and system design aspects of interest to the circuit designer. The simulator input files for the example of Fig. 5 can be found among the Saber examples provided with the Saber simulator. All of the device models used are available in the Saber template and component libraries.

The schematic of Fig. 5 consists of the switching control logic, IGBT switching devices, IGBT gate drivers, an equivalent electrical network for a motor load, and a thermal network for each IGBT. The logic circuit on the left-hand side of the network uses event-driven logic elements to implement the open-loop, sine-triangle, pulse-width-modulated control system for the switching devices. The upper right-hand side of the network includes the electro-thermal models for the power semiconductor devices (IGBTs) as well as the equivalent electrical circuit for the motor load (a motor model from the mechanical model library can also be used). The bottom of the network contains the thermal network components for the semiconductor device silicon chips, the standard TO247 power semiconductor packages, and the TTC1406 heat sinks.

B. Simulator User Interface

The interconnection of the components in the network of Fig. 5 can be specified by the user in either a netlist (list of the terminal connection points of each component of the system) or using a schematic entry program (graphical user interface with symbols for each component). Thus, the user can readily describe different electrical, thermal, mechanical, and control topologies. The DesignStar® schematic entry package was used in this work to design the electro-thermal network of Fig. 5 and to perform the simulations using the Saber simulator. The diagram in Fig. 5 is an actual printout from the DesignStar schematic entry program.

To design an electro-thermal network such as Fig. 5 and perform simulations using the DesignStar schematic entry interface: 1) the user selects components from the libraries of electrical, mechanical, electro-thermal, and thermal network components from mouse-driven menus; 2) the components are positioned and wired together using graphical mouse-driven operations; and 3) the user invokes the Saber simulator and PLTOOL post-processing waveform analysis tool to analyze the system.

Once the circuit or system is completely entered, the Saber simulator can be invoked directly from a menu within DesignStar. When transient simulation is selected, the user is prompted with a table in which the simulation time interval is specified. To view the results of the simulation, either after the simulation is complete or during the simulation, the user selects the PLTOOL plotting program from within the DesignStar environment. Within the PLTOOL graphics program, the user can then select the signals to be viewed by clicking on them with a mouse. The user can also perform mathematical operations on the simulated waveforms using the programmable waveform calculator WaveCalc™ within PLTOOL.

C. Model Libraries

Libraries of generic and characterized component models are available in Saber for control systems, power semiconductor devices, sources, digital logic, manufacturer's parts, magnetics, motors, mechanical devices and a host of other applicable parts. All of these libraries in the Saber simulator are supported with graphical symbols in the DesignStar graphical interface. The model parameters of the components within the system can be altered directly on the schematic if desired, and equations for behavioral models can also be implemented without leaving the graphical interface environment.

1) Control and Gate Driver Models. The logic gates and signal sources on the upper left-hand side of Fig. 5 implement a behavioral representation of the open-loop, sine-triangle, pulse-width-modulation control scheme. The input to the circuit is a 60-Hz sinusoidal signal which is compared with two triangle waves to produce a pair of pulse-width-modulated digital output signals. These signals are then clocked into the gate drivers of the two upper IGBTs (IGBTs 1 and 3). The clock signals are applied directly to the gate drivers of the two lower IGBTs (IGBTs 2 and 4). The models used in the control circuitry for this example contain both analog (continuous-time) and digital (logic) signals. Alternatively, a behavioral model for a commercially available PWM controller chip could be used once such a device is chosen for the application. It is also possible to employ a model of a closed-loop control system for the circuit. It general, it is much more computer efficient to utilize the behavioral models and event-driven logic models for the control circuitry when analyzing other aspects of the system.

The models for the IGBT gate drivers in Fig. 5 are also behavioral models which convert the digital inputs (logic signals) to the appropriate analog IGBT gate drive signals. In this case, the gate drive signals switch from 0 to 20 V with 50 Ω of series gate resistance. In the particular control scheme employed in Fig. 5, the bottom IGBTs are turned on continuously during one half cycle of the inverter (60-Hz cycle), while its companion device (the upper device on the opposite phase of the H-bridge) is switched at the clock frequency of the triangle waves with a varying duty cycle.

Once again, there are several levels of model representations that can be employed for the IGBT gate drivers. The drivers could be represented as discrete electrical components (i.e., transistor level). This would be useful for studying the interactions between the driver and the IGBT input characteristics. The transistor level models would also be helpful when designing new driver circuitry in terms of understanding how variations in the gate driver affect the IGBT waveforms or for designing snubber circuitry. If commercial IGBT gate driver devices are employed, then parameterized behavioral models specifically characterized for the particular gate driver device part number could be used.

2) Physics-Based Power Semiconductor Models. In the inverter of Fig. 5, IGBTs are employed as the switching devices with anti-parallel connected power diodes. However, models for other power devices such as MOSFETs or GTOs could be substituted. This allows the designer to try alternative technologies within a given topology. The model of the IGBT shown in Fig. 5 is a physics-based model capable of predicting the switching losses within the device as well as the temperature rise associated with the dissipated power. It is also possible to substitute simpler, more computer-efficient models for the devices for simulations in which the details of the switching devices are of little concern. For instance, this might be useful when designing the control circuitry or when simulating a larger system in which the inverter operates. However, the detailed physics-based models are required to determine the power dissipation and the influence of temperature on the device characteristics.

3) Mechanical and Magnetic Models. One application of an inverter is that of motor control. In Fig. 5, the load that the motor presents is represented as an inductor with series resistance. However, a more elaborate model from the Saber generic motor model library could be used. The Saber motor model library contains a variety of generic motor models for dc motors, ac induction motors, squirrel-cage motors, brushless motors, and stepper motors. In addition, mechanical element models are available that enable the user to examine the interaction of the electrical and mechanical aspects of the overall system.

Saber also provides an extensive magnetics component-modeling capability that allows the designer to develop models for custom transformers and inductors including the component geometry and detailed nonlinear properties of the core material. This is important because many of the magnetic components used in power electronic systems are at least in part custom made for the specific application. To develop models for custom magnetic components, the user specifies the number of turns on each leg of the transformer or inductor core. The transformer core may consist of one of the precharacterized cores available in the Saber component library, or a user-defined core. The user-defined core type can be modeled by specifying the geometry of the core using the core building-block models available in the Saber template library. The model for the core material can be obtained from libraries of precharacterized core materials, or the user can describe a new nonlinear core material using the generic core material models.

4) Thermal Network Modeling. The thermal network for each IGBT in Fig. 5 consists of an interconnection of thermal component models for the silicon chip, a TO247 package, and a TTC1406 heat sink. These component models describe the static and dynamic thermal impedance of each component for the full range of power dissipation levels for which the thermal components are used in practice. Using the thermal network component models, the system designer can readily examine the effects of different thermal network topologies by simply changing the connection points of the thermal terminals within the thermal network. For example, the behavior of the network in Fig. 5, including thermal coupling between adjacent IGBTs and/or power diodes mounted on the same heat sink, can be compared with the behavior of the same system, but with each power semiconductor device having a separate heat sink (as shown in Fig. 5).

As an alternative to the thermal component models, the thermal resistance and thermal capacitance element templates or the MAST® modeling language can be used to develop user defined thermal network models. This is useful for examining custom packaging systems such as multi-level hybrid packages. However, a detailed understanding of thermal network modeling [3,9] is required to develop thermal network models that are valid for transient conditions. By connecting a temperature source to the thermal terminal (T_j) of the electro-thermal semiconductor models, the electro-thermal network reduces to the traditional constant temperature circuit simulations. However, even this simplest of thermal models goes beyond the traditional SPICE-based models in which a single temperature must be specified for the entire electrical system.

IV. Electro-Thermal Analysis of PWM Inverter

The inverter of Fig. 5 is modeled, as indicated in the last section, using a mixture of behavioral blocks and very accurate physics-based models. This approach allows the study of the electro-thermal effects of the IGBT on the overall performance of the inverter. In this section, the principal operation of the inverter circuit is described along with simulation results.

A. Electrical Operation

Figure 6 shows the a) motor load current, b) IGBT 1 anode current, c) logic input signals to the IGBT gate drivers, and d) the sine-triangle control signals for the inverter of Fig. 5. The simulation of Fig. 6 is for a relatively low IGBT switching frequency (900 Hz) to illustrate the behavior of the circuit. In the PWM inverter of Fig. 5, the duty cycle of the input signal to the IGBT gate drivers is varied using the sine-triangle comparison technique to produce a 60-Hz sinusoidal variation of the motor load current.

During the positive voltage phase of the 60-Hz inverter reference signal (e.g., between 16.7 ms and 25.0 ms in Fig. 6d), the gate control signal of IGBT 1 is switched on and off at the 900-Hz triangle wave frequency, while IGBT 4 remains on. Also, during this phase IGBT 2 and IGBT 3 remain off. The inverter operation during the negative voltage phase of the 60-Hz reference sinewave is similar to that during the positive voltage phase, except that the opposite phase of the bridge is switched on and off (i.e., IGBTs 2 and 3). The sinusoidal variation of the duty cycles for IGBTs 1 and 3 are determined using gate level logic models (left-hand side of Fig. 5) to compare the magnitudes of the triangle waveforms with the magnitude of the sinusoidal reference signal. When the value of the reference sinewave is larger than the value of the upper triangle wave,

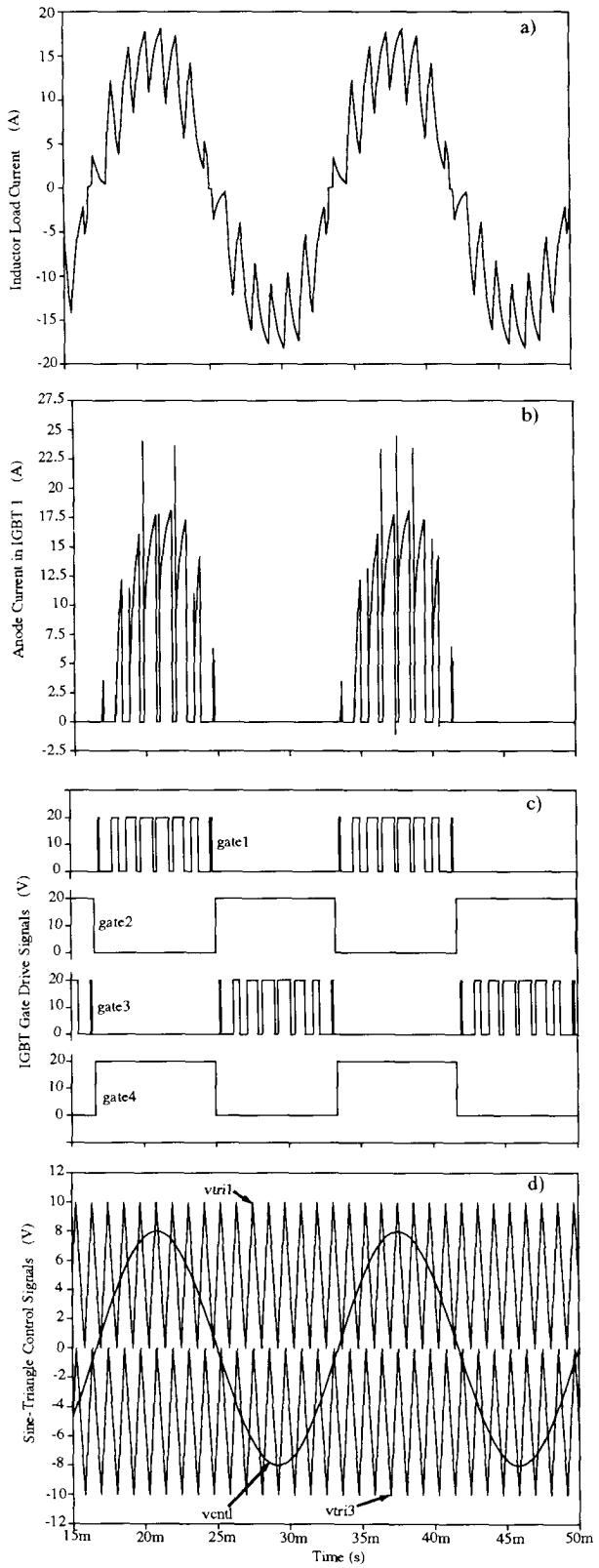


Fig. 6. Simulations of electro-thermal network of Fig. 5 for 900 Hz switching where the following curves are shown: a) motor load current, b) IGBT 1 anode current, c) logic input signals to the IGBT gate drivers, and d) the sine-triangle control signals.

the IGBT 1 gate driver signal is switched on. Otherwise, the IGBT 1 gate driver signal is off.

PWM inverters are typically operated with switching frequencies in the range of 20 kHz in order to push the switching frequency beyond the audible frequency range. A considerable amount of heat is dissipated in the IGBTs due to the on-state losses for the large motor current and due to switching losses that occur for the typical 20-kHz device switching frequency (switching frequency is 900 Hz in Fig. 6 for clarity).

Figure 7a shows the simulated load current for the 20-kHz PWM inverter operation, and Fig. 7b shows the temperature waveforms at the silicon chip surface (T_{j1}), the chip-package interface (T_{h1}), and the package-heat sink interface (T_{c1}) for IGBT 1. Notice that the silicon chip surface temperature waveform of IGBT 1 has spikes at a 20-kHz rate during the phase that the device is switching (e.g., 16.7 ms through 25.0 ms) due to the switching energy losses. Also notice that the chip surface temperature cools after the peak in load current (21 ms) and during the phase in which the device is off (e.g., 25 ms through 33 ms). The 60-Hz variations of the chip surface temperature waveform are due to the sinusoidal load current variation and due to cooling during the half of the 60-Hz cycle in which the device is off all of the time.

B. Power Dissipation and Switching Energy

Figure 8 shows the a) anode-cathode voltage, b) anode current, c) instantaneous power dissipated as heat, and d) the cumulative dissipated energy for IGBT 1 during one 20 kHz switching cycle of the simulation in Fig. 7 (i.e., the time interval between 34.136 ms and 34.148 ms). The switching cycle of Fig. 8 was chosen so that the details of both the turn-on and the turn-off waveforms can be viewed on the same graph (the on-time is much longer at the peak load current). The dissipated energy waveform is readily obtained using the WaveCalc waveform calculator to integrate the dissipated power waveform.

Immediately before IGBT 1 is turned on, the load current is flowing between IGBT 4 and the anti-parallel diode across IGBT 2 (D2). When IGBT 1 is switched on (time = 34.136 ms in Fig. 8), the load current is transferred from diode D2 to IGBT 1. In addition to the load current, IGBT 1 must also conduct the reverse recovery current for diode D2. This results in an anode current spike at turn-on that is larger than the on-state current. The IGBT on-state current for the switching cycle of Fig. 8 is approximately 3.5 A (the on-state current is approximately 16 A for the switching cycle at the peak load current in Fig. 7). Because IGBT 1 is forced to bear the full supply voltage of 300 V and a current that is larger than the load current during the reverse recovery of diode D2, a short-duration, high-power dissipation spike exists at turn-on. This results in the turn-on energy indicated in Fig. 8d ($E_{sw,on}$=70 μJ/cycle). In practice, this turn-on energy can be reduced by using a larger IGBT gate resistance or using a more advanced control strategy.

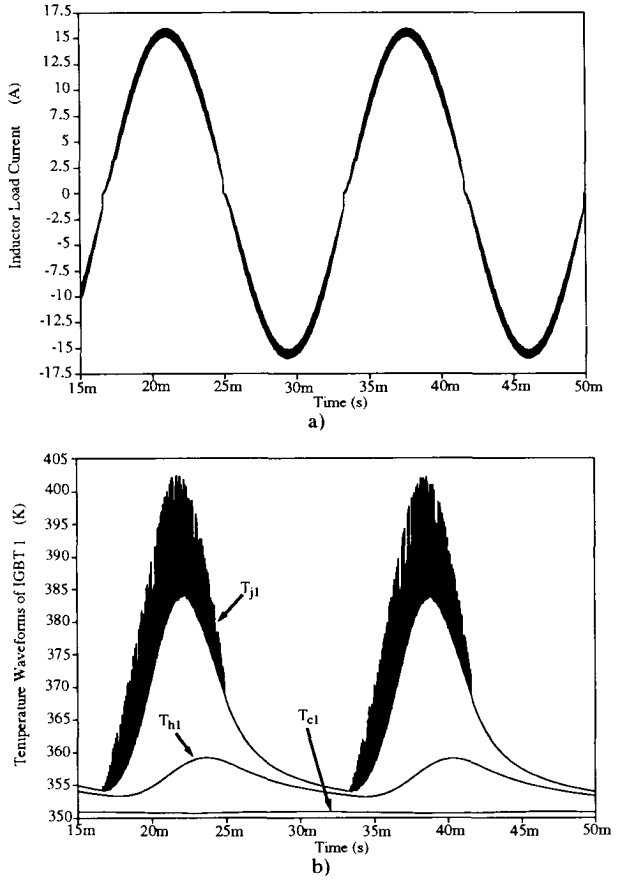


Fig. 7. Simulations of Fig. 5 with a switching frequency of 20 kHz where a) is the load current and b) is the temperature waveforms at the silicon chip surface (T_j), the chip-package interface (T_h), and the package-heat sink interface (T_c) for IGBT 1.

Once the reverse recovery of diode D2 is nearly complete (after the so-called T_A phase of the diode recovery [11]), the anode-cathode voltage of IGBT 1 drops (cathode voltage rises) and approaches the IGBT on-state voltage. Once the device is fully on, the power dissipation is determined by the product of the on-state voltage and the load current. During this on-state phase of the switching cycle (e.g., 34.136 ms through 34.148 ms), the power dissipation is small compared to the value of the power spikes during switching events, but the time duration of the on-state phase of the switching cycle is much longer than the switching times. Therefore, the energy loss waveform rises with a constant slope (determined by the load current and the IGBT on-state voltage) during the on-state phase of the switching cycle.

When the gate of IGBT 1 is turned off (34.148 ms in Fig. 8), the anode-cathode voltage rises to maintain the constant current in the load inductor. Once the anode-cathode voltage reaches the supply voltage (300 V), the anode voltage is clamped at the supply voltage by the anti-parallel diode on IGBT 2. Then, the anode current initially drops rapidly followed by a less rapidly decaying current tail due to the stored charge in the base region of the IGBT. As the IGBT anode current is removed, the diode D2 begins to conduct to maintain the constant load inductor current. During the time

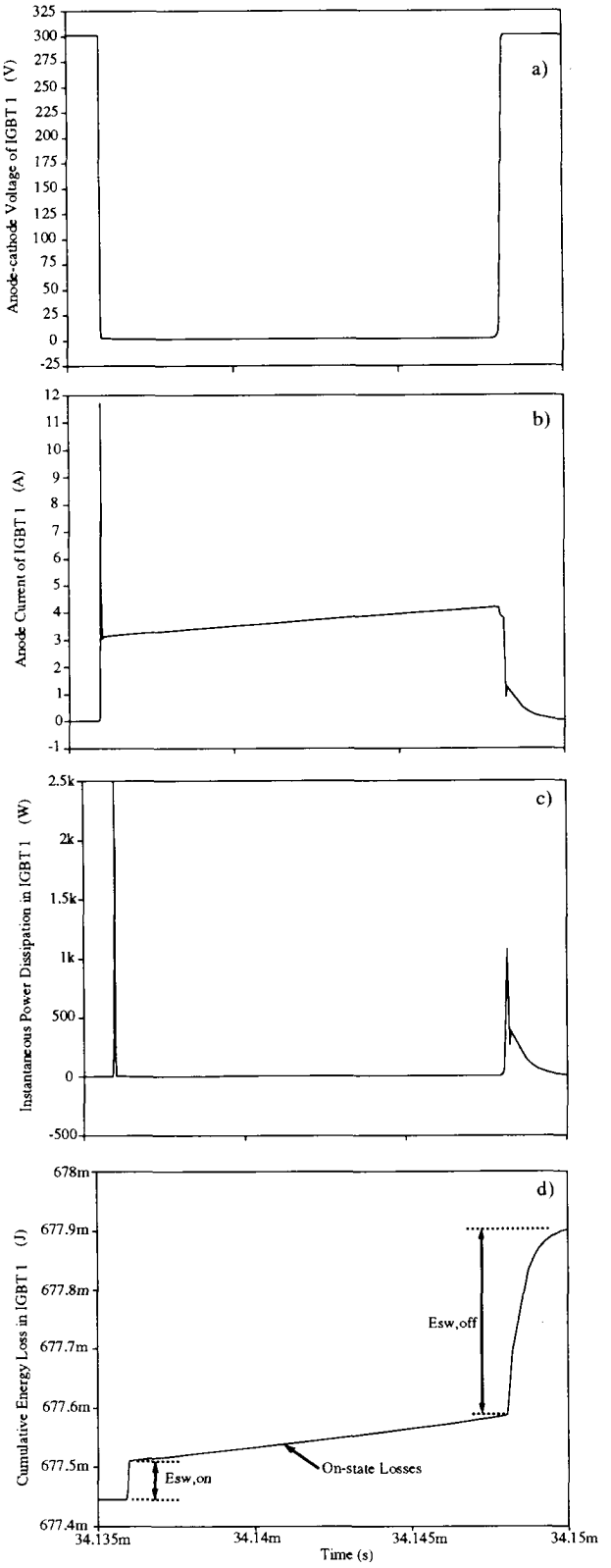


Fig. 8. One switching cycle from the 20.1 kHz simulation for the a) anode-cathode voltage, b) anode current, c) instantaneous dissipated power, and d) the cumulative dissipated energy for IGBT 1.

that the IGBT anode voltage is rising, the anode current is equal to the inductor current, and during the time that the IGBT current tail decays, the anode voltage is equal to the supply voltage. Thus, a large anode-cathode voltage and a large anode current exist simultaneously resulting in a spike of a high power dissipation level. Although the power dissipation level is not as high as during the turn-on event, the turn-off switching time is much longer due to the slowly decaying excess carriers in the bipolar transistor base. Thus, the turn-off switching energy indicated in Fig. 8d ($E_{sw,off}$) is larger than the turn-on switching energy.

C. Response of Thermal Network

From the temperature waveforms of Fig. 7b, it is evident that the thermal response of the silicon chip determines the IGBT temperature variations during the device 20-kHz switching cycle (from 385 K to 405 K), because the temperature at the package header (T_h) does not change during the 20-kHz cycles. The thermal response of the silicon chip and TO247 package determines the device temperature variations during a single phase of the 60-Hz sinusoidal output (from 355 K and 385 K), because the temperature at the package case (T_c) does not change. For the relatively high frequencies of the electrical network (high frequency with respect to some of the time constants of the thermal network), the temperatures within the heat sink do not change substantially. However, the heat sink does influence the thermal response to changes in the power dissipation level over longer periods of time such as during the system start-up or during load impedance changes.

For the inverter of Fig. 5, approximately 20 minutes of real time (not simulation time) is required for the heat-sink fin temperatures (T_{fin}) to reach a steady-state condition. Thus, a simulation of the complete thermal start-up condition would take an inordinate amount of simulation time for the 20-kHz inverter operation. Therefore, it is beneficial to separate the simulation of the thermal response to the low frequency components of the power dissipation function from the simulation of the response to the high frequency components. To do this, a power source equal to the average power in each of the IGBTs is connected to the same thermal network arrangement as in Fig. 5, but without the electrical network: 1) The average power can be calculated using the waveform calculator to integrate the power dissipation in the IGBT over a single switching cycle of the inverter, and then dividing by the time interval of the switching cycle, 2) A transient simulation is then performed for the thermal network to determine the thermal response to the changes in the average power dissipation level.

For example, Fig. 9 is a simulation of the low frequency components of the temperature waveforms at the silicon chip surface, the chip-package interface, the package-heat sink interface, and the heat sink fin for IGBT 1 during the start-up of the inverter in Fig. 5. For the simulation of Fig. 9, the initial conditions for the temperature throughout the thermal network is 300 K and the power dissipation level steps from zero to 15.3 W at time = 0. Although the chip and package temperature waveforms respond rapidly to the change in power dissipation level at start-up, the temperatures within the heat sink respond much more slowly. Approximately 10 seconds is required for the heat to diffuse to the heat-sink fin. For longer times, the thermal response of the heat sink is determined by the total heat capacity of the heat sink and the nonlinear convection heat transfer at the heat-sink fins. The high-frequency components of the thermal response (as described above for Fig. 7) can be combined with the low-frequency components by using the temperature distribution at any point in Fig. 9 as an initial condition for the full electro-thermal simulation. This can also be used to periodically recalculate the dissipated power and restart the transient simulation to include electro-thermal interactions as described below.

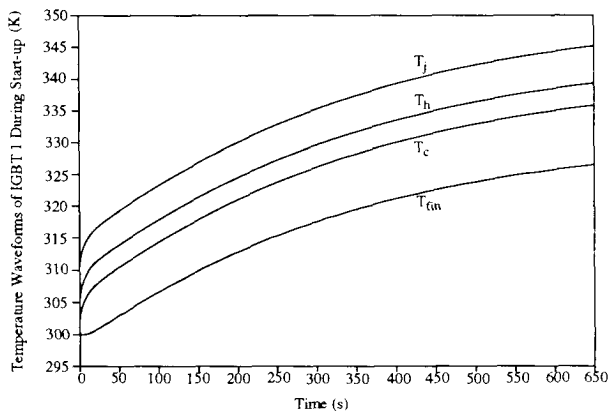


Fig. 9. Simulated thermal response at start-up for the average power dissipated in IGBT 1 indicating the temperature at the chip-package interface, the package-heat sink interface, and the heat sink fin.

D. Electro-thermal Interactions

For the steady-state thermal response shown in Fig. 7, the temperature at the package-heat sink interface (T_c) was determined to be 51 K above the 300-K ambient temperature. Because the IGBT electrical characteristics change with temperature, the average power dissipation level changes as the heat sink temperature rises. To account for this, a five step iterative process is used to determine the initial condition of the temperature for Fig. 7:

1) First, a full electro-thermal simulation of the inverter is performed over a few 60-Hz cycles (three in this case).

2) The average dissipated power is determined for each device using the WaveCalc™ waveform calculator to integrate the dissipated power over a complete 60-Hz cycle.

3) The calculated value of average power is then used as a power source into the corresponding thermal network of Fig. 5 without the electrical network.

4) A dc analysis is performed for the thermal network to determine the average steady-state temperature of the device using the calculated average power dissipation in each device.

5) Finally, the average steady-state temperatures are used as an initial condition for another full electro-thermal simulation in step 1.

This iterative process is repeated until the average power converges to steady state. Three iterations were required for this circuit to determine that the average power dissipation of the upper IGBTs is 20.5 W, while the lower devices dissipated about 15 W.

Figure 10 shows the simulated energy losses neglecting the device self-heating for the same time interval as in Fig. 8d. This simulation was performed using the electrical network of Fig. 5, but with the thermal terminals of the IGBTs connected directly to the 300-K constant temperature source. The turn-off energy for the switching event that occurs at 34.148 ms changes from 0.3-mJ/cycle including the self-heating (Fig. 8d) to a value of 0.15 mJ/cycle for the constant temperature simulation of Fig. 10. This occurs because the excess carrier lifetime (τ_{HL}) increases with increasing IGBT temperature [8]. In addition, the on-state energy increases with temperature for the high current range of the inverter cycle due to the decrease in transconductance with increase in temperature [8]. For the $\tau_{HL} = 0.3$ μs device used in this paper the cumulative on-state energy losses are approximately equal to the cumulative turn-off switching energy losses.

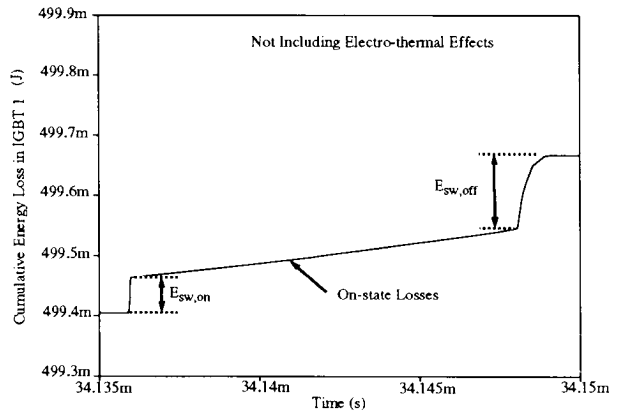


Fig. 10. Simulated energy loss neglecting the device self-heating (i.e., IGBT temperature is constant at 300 K) for the same time interval as in Fig. 8d.

The full electro-thermal simulation described in this paper is required to accurately predict the total energy loss and the overall efficiency of the inverter network of Fig. 5. The average power dissipation in IGBT 1 calculated including the device self-heating is 20.5 W, whereas the value calculated assuming a constant temperature of 300 K is much less, 15.3 W. The overall efficiency for the PWM inverter can be calculated by integrating the power dissipated in the load resistor over a complete 60-Hz inverter cycle, and dividing by the integral of the power out of the 300-V power supply. The overall energy efficiency calculated for the simulation including the self-heating effects is 96.1%, whereas the constant temperature simulations effectively neglect 15% of the total energy loss in the inverter. Because the simulations including self-heating accurately describe the dissipated power, the simulations can be used to select an IGBT type that minimizes the energy losses and to design a thermal management system that is suitable for the calculated power dissipation levels.

V. Conclusions

The recently developed electro-thermal network simulation methodology described in this paper is used to analyze a full wave IGBT PWM inverter. In this analysis, the instantaneous temperature of the IGBT is determined for the actual circuit use conditions of the PWM inverter, and the influence of this thermal response on the electrical behavior of the PWM inverter is also determined. This is an important capability because the cost of the thermal management of electronic systems depends heavily upon the efficiency of the circuit design and because the self-heating of the semiconductor devices can affect the operation of the electronic circuit. Techniques have also been developed to simulate the steady-state large signal response of the system using the Saber waveform calculator to periodically integrate the dissipated power over a single 60-Hz cycle. It is shown that the thermal response of the silicon chip determines the IGBT temperature rise during the device switching cycle, the thermal response of the device TO247 package and silicon chip determines the device temperature rise during a single phase of the 60-Hz sinusoidal output, and the thermal response of the heat sink determines the device temperature rise during the system start-up and after load impedance changes.

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