Characterization of Power Electronics System Interconnect Parasitics Using Time Domain Reflectometry

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***Abstract*—The significance of interconnect parasitics of power electronics systems is their effects on converters' electromagnetic interference (EMI)-related performances, such as voltage/current spikes, $dv/dt, di/dt$, conducted/radiated EMI noise, etc. In this paper, a time domain reflectometry (TDR) measurement-based modeling technique is described for characterizing interconnect parasitics in switching power converters. Experiments are conducted on power components of a prototype high-power inverter, including insulated gate bipolar transistor (IGBT) modules, busbar, and bulk capacitors. It is shown that the interconnect inductance of the IGBT module can be extracted completely using TDR. It is also shown that the busbar equivalent circuit can be modeled as transmission line segments or L–C filter sections, and the bulk capacitor contains a significant equivalent series interconnect inductance.**

***Index Terms*— Device packaging, IGBT model, interconnect parasitics, power inverter, time domain reflectometry.**

I. Introduction

THE SIGNIFICANT effects of interconnect parasitics of power electronics systems are on converters' electromagnetic interference (EMI)-related performances, such as voltage/current spikes, voltage/current slew rate (i.e., dv/dt or di/dt), conducted/radiated EMI noise spectrum, etc. For example, dv/dt and di/dt are of great concern in pulsewidth-modulated inverter-fed motor drive systems due to motor winding insulation voltage rating, and motor bearing leakage current [1]–[3]. The dv/dt is also thought to be one of the major causes of common-mode noises generated by inverters. In recent years, EMI considerations are becoming increasingly important, as the electromagnetic compatibility (EMC) regulations (typically defined from 10 kHz to 30 MHz) have become more stringent [4], [5]. Most of the current EMI-related designs use experimental trial-and-error methods, which are time consuming and difficult to use in optimizing the designs. Hence, it is desirable that the EMI characteristics of power converters be analyzed and predicted at the early design stage. Characterization of interconnect parasitics provides important information for identification of the causes of EMI noise and for optimization of converters' design and layout.

Interconnect parasitics are mainly related to device packaging and circuit layout. Parasitics exist in all kinds of elements of power converters, such as electronic IC's, power device modules, capacitors, magnetic components, PCB traces, busbars, wiring cables, and connectors, etc. They may significantly affect the converter's performance in EMI aspects. Particularly, a variety of parasitic inductances seem to be the major concern.

Much research effort has been reported on methods of extracting parasitic parameters [6]–[11]. Although many different methods have been proposed, they can be divided into two categories: the three-dimensional (3-D) finite-element analysis (FEA) [6], [7] and the partial element equivalent circuit (PEEC) method [8]–[11]. Some software tools (e.g., InCa) have been developed using the above methods. However, both FEA and PEEC methods are purely mathematical computation/simulation approaches. For example, in InCa, a parasitic inductance is calculated according to the geometrical structure of the conductor segment under investigation, assuming that the physical parameters of the conductor are known. In these methods, there are some fundamental limitations, which can be summarized as below.

1) The physical properties, parameters, and structure of the conductor materials in computation are selected by assumption or *a priori* instead of by measurement. In most cases, it is difficult to select the correct values. Moreover, some connections may consist of nonuniform medium, or may have characteristic discontinuities (e.g., as a result of welding or soldering process), which are difficult to identify.
2) Leads or wire-bond interconnects inside power device modules or passive components are almost impossible to calculate accurately because they are physically inaccessible after being packaged; therefore, neither the material nor the geometry can be well identified or understood. In fact, the geometry is very irregular in most cases.

In this paper, a measurement-based modeling technique is used to characterize major interconnect parasitics of a typical high-power converter. This technique employs the time

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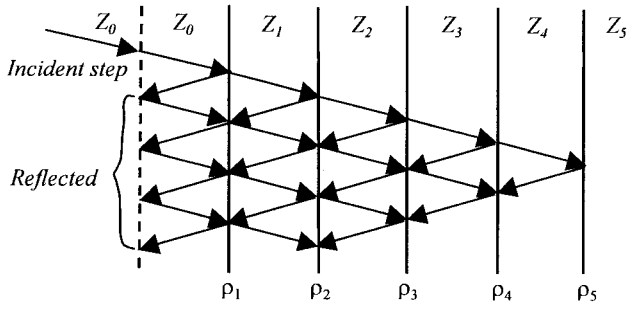

Fig. 1. Incidental step signal and its reflected responses.

domain reflectometry (TDR) measurement approach, which has been proposed for characterization of lead or interconnect parasitics in electronic integrated circuit (IC) packages and has been developed as a commercial instrumentation tool [13]–[16]. In Section II, the TDR method is briefly reviewed, the instrumentation setup is introduced, and the modeling procedures are also described. In Section III, experimental results using TDR are shown on typical elements of a prototype high-power inverter [12], including an insulated gate bipolar transistor (IGBT) module, a custom-manufactured busbar, and a bulk capacitor. Finally, the conclusion and discussion of this paper are given in Section IV.

II. TDR Method

A. TDR Principle

The TDR method is based on transmission line theory, which has existed for several decades. Radar detection technique is developed from the TDR method and has successfully been used. However, it was only a few years ago when TDR became a commercially available tool for measurement and modeling of lead or interconnect parasitics in electronic IC devices [13]–[16].

The TDR technique is a measurement-based modeling approach rather than a traditionally pure mathematical tool. According to the transmission line theory, when an electrical signal travels through the media of a conductor, it is partially reflected as it encounters impedance mismatches along the path, as shown in Fig. 1. The media can be viewed as a series of conductive planes. The signal gets reflected at each plane and some of it may travel back to the source. The theory goes that, the reflection coefficient ρ_i, which is defined as the ratio of the reflected voltage to the incident voltage, is simply determined by the media impedances Z_i at the reflection plane, i.e.,

$$\rho_i = \frac{Z_i - Z_{i-1}}{Z_i + Z_{i-1}}.$$

As can be seen from Fig. 1, when an incident step voltage is injected into the media, the signal reflected at different planes arrives back to the source with a different time delay. Hence, the impedance profile or Z profile, defined as the varying impedance along the signal path, can be computed if the reflected signal with respect to delay time is measured. There are actually quite a few algorithms to do this. Moreover, the obtained Z profile should then provide a visualization of the impedance of the signal path, so that the waveform features can

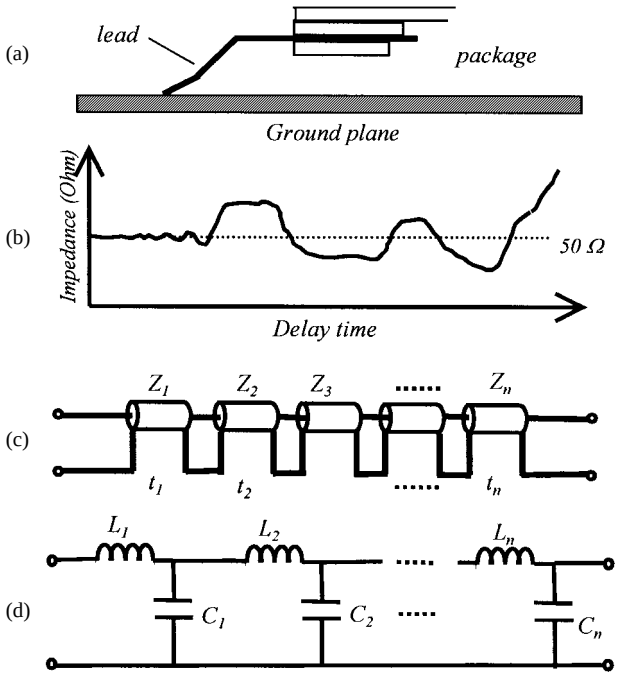

Fig. 2. A lead can be viewed as transmission line segments and modeled as L–C sections of varying impedance.

be readily associated with the physical features of the signal path. In fact, multiple reflections may occur, which further complicate the analysis. However, they can be taken care of using certain Z-profile computation approaches, such as the inverse scattering algorithm. To take the nonideality of the voltage step pulse into consideration, the so-called direct dynamic deconvolution or layer peeling algorithm is preferred [17].

Therefore, any electrical conductor, for example, a lead in a package as shown in Fig. 2(a), can be modeled as a distributed transmission line with varying impedance along its path, as shown in Fig. 2(b), and can be measured by TDR. In general, it is not practical to use a distributed transmission line model. It is desirable that the model be reduced to a string of transmission line segments with reasonable approximation, as shown in Fig. 2(c). Each segment acts as a short uniform transmission line, having a time delay (T_d) and characteristic impedance (Z_o). The delay and impedance mainly depend on several factors including the length of the segment, its proximity to metal surfaces, and its dielectric properties. In practice, the segments are partitioned on the Z-profile curve and their impedance and time delay are calculated by averaging. Moreover, individual transmission line segments can be approximated as low-pass L–C filter sections as indicated in Fig. 2(d) using

$$L = T_d \cdot Z_o \quad C = T_d / Z_o.$$

The inductance can also be computed directly by

$$L = \tfrac{1}{2} \int_{t1}^{t2} Z(t)\, dt$$

and the capacitance by

$$C = \tfrac{1}{2} \int_{t1}^{t2} \frac{1}{Z(t)}\, dt$$

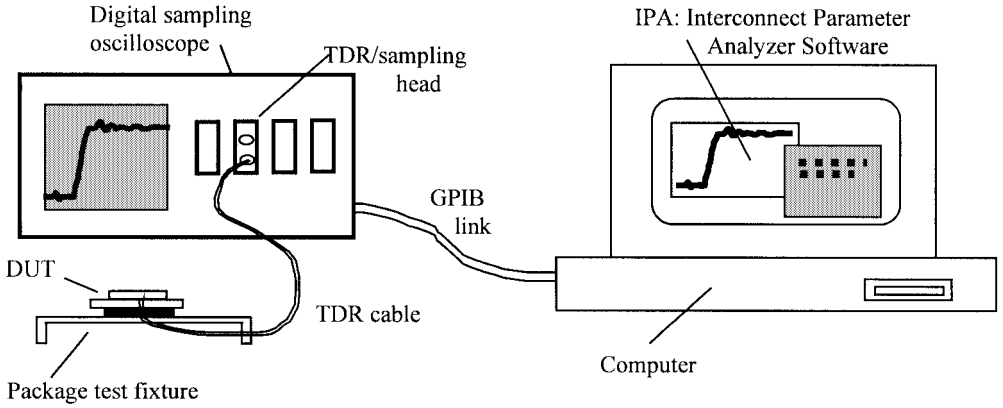

Fig. 3. Instrumentation setup of Tektronix TDR system.

where t_1 and t_2 correspond to, respectively, the beginning and the end of the interval over which L and C are evaluated on the Z-profile curve. Furthermore, a lumped L–C model can thus be obtained by combining the inductance and capacitance into fewer sections.

The TDR method can also be applied to modeling multiple coupled conductors and ground bouncing [13]–[15].

B. TDR Instrumentation

The basic TDR instrumentation setup is comprised of a Tektronix 11 801A digital oscilloscope, TDR/sampling head, 50-Ω coaxial cable, device test fixtures, computer, and interconnect parameter analyzer (IPA) software as shown in Fig. 3. The TDR/sampling head generates an incident voltage step signal and samples the reflected voltage waveform. Both the incident and the reflected waveforms need to be captured by the digital oscilloscope and sent to the computer for processing.

Z-profile algorithms are implemented in the IPA software. The IPA tool is used to compute the impedance profile from the captured data. It allows users to do segment partitions on the Z-profile curve and choose a proper type of model from its model library for each individual segment. Parameters of each model are extracted by the software. Also, the parameters can be modified manually for trial-and-error purposes. The more segments are partitioned, the more accurate the model becomes. However, a model with too many segments is not very useful due to the complication and computing burden it incurs in simulations. There are several kinds of models available in the library, such as single lumped models (single transmission line, L, C, or single L–C filter), coupled lumped models (coupled transmission lines, coupled L's, or coupled L–C sections), etc. The derived segment model may need to be simplified with fewer segments. It is up to the users regarding which model to choose, how many segments to use, or how to interpret the model derived.

The obtained model still needs to be verified and its parameters may need to be adjusted. The verifying procedure is to compare simulations of the model with actual measurements. For this purpose, PSpice is incorporated into the IPA software. The captured incident voltage step waveform is applied to the model (segment transmission line or L–C model, or a combination of both) and the reflected response is simulated using PSpice. Then the measured and simulated response waveforms can be overlaid on the screen for direct comparison. If they do not match well, one should either manually adjust the parameter values of the segment models or modify the segment partitions on the impedance curve and redo the model parameter extraction. Such a matching process should be repeated until the simulation response matches well with the measured one.

III. Experimental Results

TDR modeling experiments are conducted on typical power stage elements of a prototype high-power inverter [12], including a half-bridge IGBT module, custom-manufactured busbar, and bulk capacitor. Experimental procedures and the major results are given in the following three sections.

A. IGBT Module Interconnects

Fig. 4 shows an opened module of the tested IGBT device and its equivalent circuit, having complete half-bridge switches in one package. As described above, it is of great importance for an EMI-related investigation to find all the major parasitic inductance of the leads and interconnects in the module. Therefore, the segment models of the leads and interconnects obtained from the TDR measurements are approximated as single lumped inductances. Although these approximations reduce the accuracy of the fit to the TDR signal, it is desirable to have a simplified model that is accurate over the full range of application conditions in which the model will actually be used.

As can be seen in Fig. 4, the IGBT module has four terminals for the gate circuit (i.e., $G1$, $E1$, and $G2$, $E2$) and three power stage connection ports (i.e., $C1$, $E2$, and $C2/E1$). Each of the terminals or power ports has an inherent parasitic lead inductance. In addition, there should be another parasitic inductance due to internal interconnect between emitter of $Q1$ and collector of $Q2$, which can be observed on the open module, but cannot be seen on the photograph. Such an internal interconnect should also exist in any other dual-device IGBT module. So there should be a total of four parasitic inductance variables in the power circuit and four in the gate control circuit. Next, it is shown that interconnect inductances of the power circuit and those of the gate circuit can be modeled separately. The diagram showing all of the interconnect inductances of the IGBT module is then developed according to the above observation.

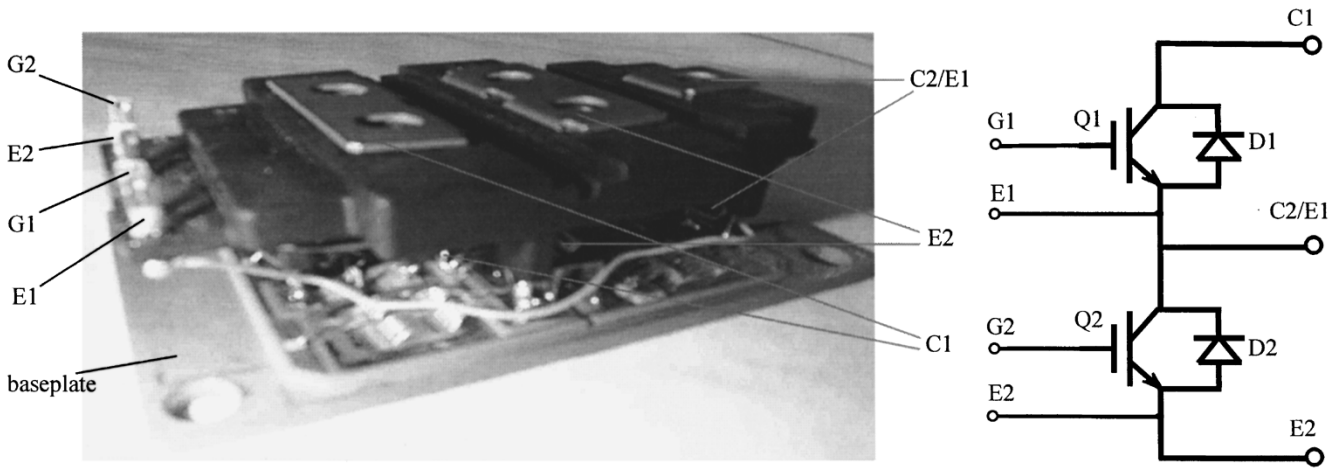

Fig. 4. A 600-V/400-A half-bridge IGBT module and its equivalent circuit diagram.

First, the total equivalent inductance of the interconnect paths between each pair of the three power ports (i.e., from $C1$ to $E2$, from $C1$ to $C2/E1$, and from $E2$ to $C2/E1$) are obtained by measurement and computation. Then the partition of each parasitic inductance of the power circuit is done with the assumption that the inductance of lead $C1$ and that of lead $E2$ are the same. This assumption is based on the observation that the two leads are very similar in structure and in material. In addition, it is shown that the total inductance of the two leads is small, and thus it is not unreasonable to assume they are equal.

Second, measurements are conducted to obtain the total equivalent inductance along each gate signal paths (i.e., from $G1$ to $E1$ and from $G2$ to $E2$). In order to determine each lead inductance from the total value for the pair, additional measurements are performed by applying the incident voltage step signal on each of the four gate lead terminals with respect to the base plate of the module. The inductance along each of the signal paths is computed with respect to the base plate as the ground plane. The ratio of the lead inductances with respect to the base plate are then used to factor out the inductance of each lead from the measured value of the lead pair inductance, e.g., $L_{G1} = L_{G1_{E1}} \cdot (L_{G1-B}/L_{E1-B})$.

From the TDR measurements between the power ports ($C1$, $E2$, and $C2/E1$), the impedance profiles are computed using the IPA software. The waveforms shown in Figs. 5–7 are the Z profiles of the interconnect pairs from $E2$ to $C2/E1$, from $C1$ to $E2$, and from $C1$ to $C2/E1$, respectively.

To perform the measurements, the TDR/sampling head is connected to the IGBT module terminals or ports using a coaxial cable (with an SMA connector) and a test fixture, which is made to adapt to the IGBT module. The test fixture is designed to have a similar ground plane configuration to application conditions, but to launch a clean signal from an impedance near that of the 50-Ω cable. To interpret the Z profile, Fig. 5 is used as an example. The Z profile pertaining to the conductor properties along the signal path, as indicated in Fig. 5, can be partitioned into several segments.

The impedance curve in Fig. 5 starts with a 50-Ω straight line representing the coaxial cable. It continues with some oscillations due to the transition from the SMA connector to the

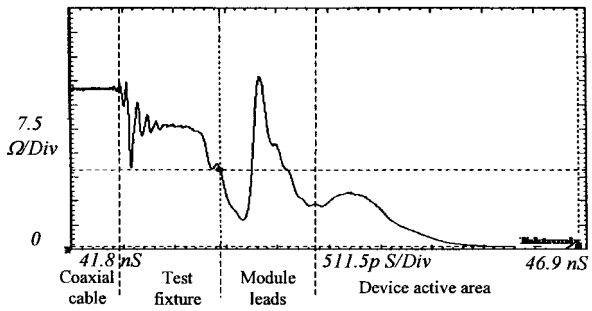

Fig. 5. Z profile of interconnect from $E2$ to $C2E1$.

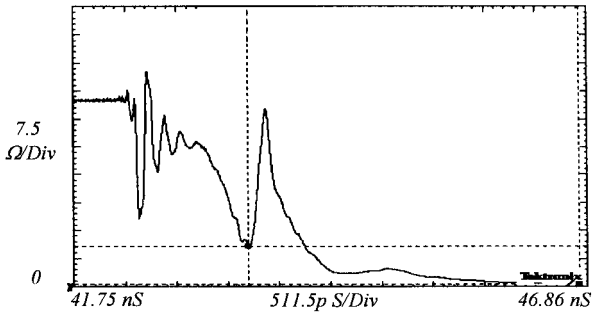

Fig. 6. Z profile of interconnect from $C1$ to $E2$.

striplines in the test fixture. The Z-profile curve continues with another flat portion showing the striplines of the test fixture. The curve then has a large peak due to the interconnects in the package. Finally, the Z-profile curve approaches zero as the signal approaches the device active area, because the IGBT output capacitance is large enough to appear as a short circuit to high frequency of the TDR signal.

By integrating the impedance curve and its reciprocal over the lead section in Fig. 5, the total lumped inductance and capacitance from $E2$ to $C2/E1$ are then calculated as 17.5 nH and 55 pF, respectively. The capacitance is small enough that it can be neglected, and the lead can be modeled as a single inductance.

In a similar manner, from Figs. 6 and 7, the total equivalent inductance along the other two paths can be extracted as 10.6 nH which contains the inductance from $C1$ to $E2$ and 23.1 nH which contains the inductance from $C1$ to

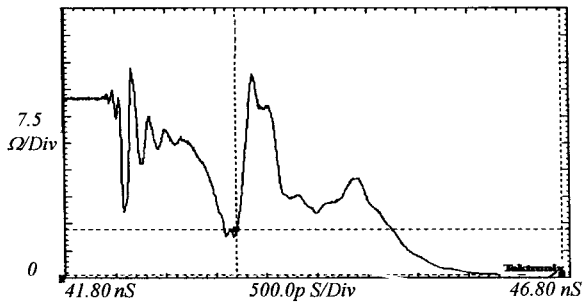

Fig. 7. Z profile of interconnect from $C1$ to $C2E1$.

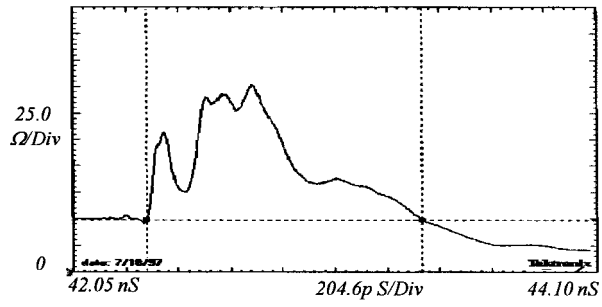

Fig. 8. Z profile of gate lead from $G1$ to $E1$.

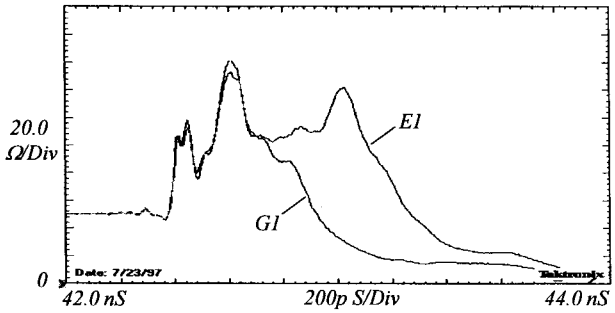

Fig. 9. Comparison of Z profiles: lead $G1$ versus $E1$ with respect to the base plate.

$E1$, respectively. Using these three inductance values, each of the interconnect inductance can be calculated under the aforementioned assumption that leads $C1$ and $E2$ have the same amount of inductance. Thus, the parasitic inductance of power circuit is completely modeled, as indicated in Fig. 12 where L_{E1} represents the inductance of the internal connection between the emitter of $Q1$ and collector of $Q2$.

Similarly, the gate lead parasitics are also characterized. The impedance profile measured from $G1$ to $E1$ is shown in Fig. 8. From Fig. 8, the total gate lead inductance of device $Q1$ is computed as 41 nH which includes the inductance of gate lead $G1$ and that of gate lead $E1$. To determine their individual inductance, additional TDR measurements are conducted on each of the two gate lead terminals with respect to module baseplate. The results are shown in Fig. 9 where the inductance from $G1$ to the baseplate is evaluated as 22 nH and that from $E1$ to the baseplate 34.5 nH. This inductance ratio is used to factor out the individual lead inductance from the total inductance. It is noted that the sum of these two-lead inductance values is a little greater than the measured total inductance of the lead pair. However, this can be attributed to the nonideality of the module baseplate which has a certain amount of inductance.

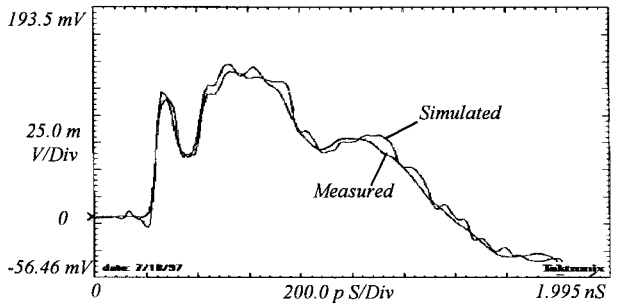

Fig. 10. Simulated versus measured TDR responses from $G1$ to $E1$.

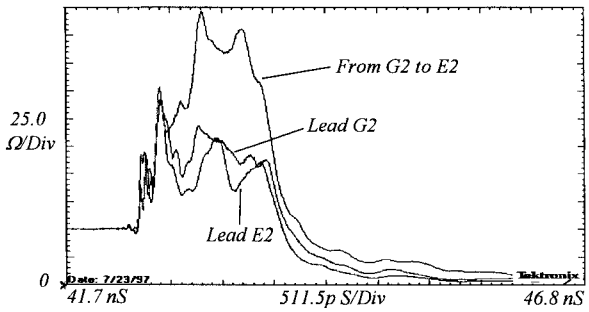

Fig. 11. Z profiles measured on gate leads of $Q2$.

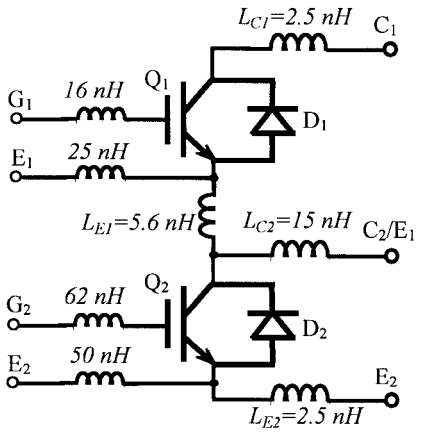

Fig. 12. Interconnect inductance of the IGBT module.

Shown in Fig. 10 is an example comparison of the simulated reflected response with the measured TDR response from $G1$ to $E1$. A model of six L–C filter sections in cascade is used in the simulation. It can be seen that with the six-segment approximation the results are in a good match.

The procedure of characterizing the gate lead inductance of $Q2$ is the same as that described above for $Q1$. Shown in Fig. 11 are the measured three Z profiles: from $G2$ to $E2$, from $G2$ to the baseplate and from $E2$ to the baseplate. The total inductance is computed as 112 nH. The partitioning result is that the equivalent inductance of leads $G2$ and $E2$ are 62 and 50 nH, respectively.

B. Busbar Interconnect

A busbar shown in Fig. 13 which was custom designed for use in the prototype three-phase inverter has been characterized using TDR. The busbar is to be used to connect the dc power source and the three IGBT inverter output legs. As can be seen in Fig. 13, the busbar has three sets of bushings

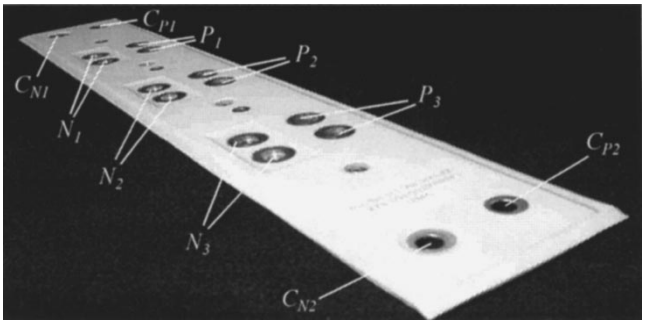

Fig. 13. The custom-designed busbar tested in experiment.

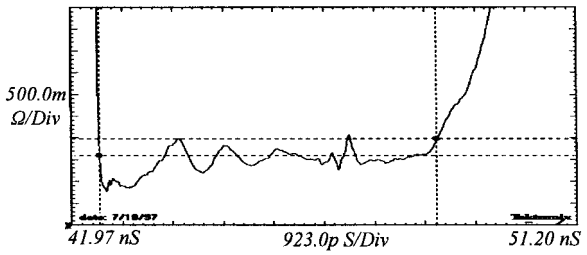

Fig. 14. Z profile of the busbar with open end.

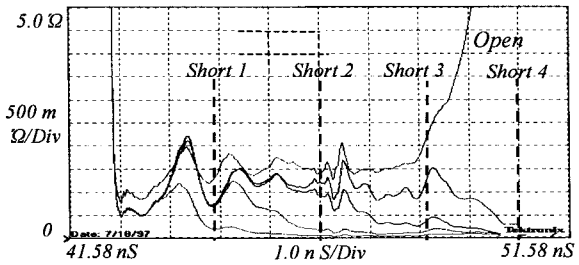

Fig. 15. Z profiles of the busbar with different shorts.

in the middle which are for connection to the three IGBT modules and two holes at both ends for connection with the bulk capacitors. The insulation contains 2-mil mylar, 3-mil tedlar, and 2-mil adhesive material.

By injecting the incident signal to the capacitor bolt holes at one end of the busbar, the impedance profile of the busbar with the other end open is shown in Fig. 14. As can be seen, the busbar is like a transmission line, with an average impedance of 1.5 Ω and a total time delay of 3.0 ns.

Along the busbar, there are four sets of bolt holes in addition to the one end where the TDR signal is injected, which divide the busbar into four equal length segments. To show the visualization feature of TDR method, a group of impedance profiles with a short circuit at each of the bolt holes are shown in Fig. 15. It can be seen that each impedances profile drops to zero at the position where it is shorted. The transmission line model and lumped parameter model of the busbar are shown in Fig. 16, indicating the connecting points for each of the three modules and the two capacitors. Each transmission line segment can be approximated by an L–C filter of 1.25 nH and 0.55 nF.

C. Bulk Capacitor Interconnect

The measured impedance profile of a 2700-μF 600-V electrolytic capacitor is shown in Fig. 17. The profile has a large

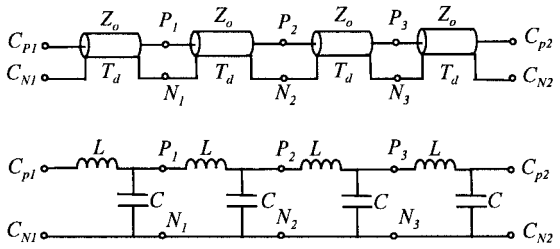

Fig. 16. Equivalent models of the busbar.

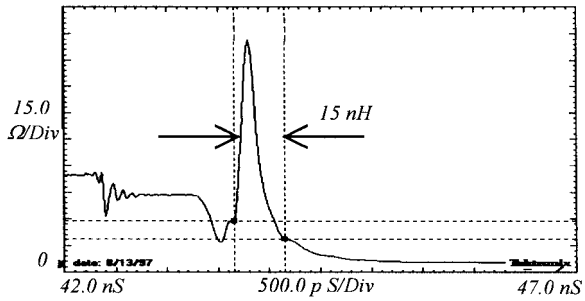

Fig. 17. Z profile of the capacitor interconnect.

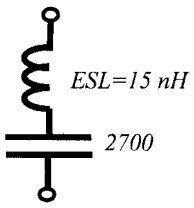

Fig. 18. Leakage inductance of the capacitor.

spike in a short period of time representing the leakage inductance. The curve drops slowly after the spike because it takes a long time to charge the capacitor. The total parasitic inductance is evaluated as 15 nH. Thus, the capacitor can be modeled by the equivalent circuit shown in Fig. 18.

IV. Conclusion

This paper has described the use of the time domain reflectometry-based modeling technique to characterize interconnect parasitics in switching power converters. Experiments were conducted on typical power stage elements of a prototype high-power inverter, including an IGBT module, custom-manufactured busbar, and bulk capacitor. It is shown that the parasitic inductance of the leads and interconnects of the module can be characterized completely using TDR. It is also shown that the busbar has an equivalent circuit model of transmission line segments or L–C filter sections, and the capacitor has a significant interconnect inductance. Moreover, the TDR method may also be used to characterize any other power electronics devices or components. In addition, the authors believe that all major causes of EMI noise can be identified and EMI-related performance predicted by analysis and simulation using the TDR technique, together with the physics-based IGBT model [18], [19].

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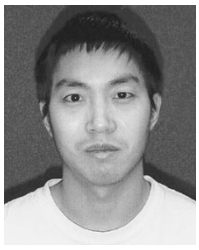

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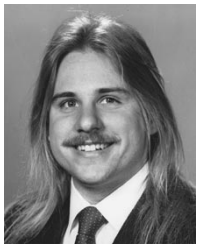

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