Automatic Inductive Voltage Divider Bridge for Operation from 10 Hz to 100 kHz

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Abstract—A bridge to calibrate programmable and manual inductive voltage dividers is described. The bridge is based on a programmable 30 b binary inductive voltage divider with terminal linearity of ± 0.1 ppm in phase and ± 2 ppm quadrature at 400 Hz. Measurements of programmable test dividers can be automated using software developed to align the bridge components and perform an automatic balance.

I. INTRODUCTION

INDUCTIVE voltage dividers (IVD's) and bridges to compare them have been extensively described in the literature. Most of the work has concentrated on manually operated, decade IVD's for use in the low audio frequency range [1]–[4], with some mention of operation at higher frequencies [5]. In the late 1960's, Hoer described a fixed ratio binary inductive voltage divider (BIVD) designed to operate at 1 MHz [6]. Consequently, several programmable BIVD's were developed for use in automatic measurement systems [7]–[9]. Further development was motivated by the need for a system to support new commercial programmable IVD's.

The BIVD-based bridge described in this paper was originally developed to calibrate specific ratio ranges of a programmable IVD used for temperature control in the Zeno project (a fluid dynamics experiment scheduled to fly on the Space Shuttle in 1993 [10]).

II. INDUCTIVE VOLTAGE DIVIDER BRIDGE

The primary objective of the new bridge is to automate IVD calibrations rather than to improve accuracy. With this in mind, we adopted an approach that made use of commercial instrumentation where possible.

A programmable, digitally synthesized, sine-wave generator was selected as the voltage source for the IVD bridge, which is shown schematically in Fig. 1. This source produces two amplitude- and phase-adjustable sine waves from 10 Hz to 100 kHz. Channel A of the voltage source supplies the sinusoidal test voltage V that is isolated through transformer T_I . Channel B supplies a second sinusoidal voltage that is in quadrature with V and programmable in amplitude. The Ref output is a TTL signal

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that is in phase with the Channel A signal and provides the reference signal for the detector. The detector is isolated from the measurement point (the tap of the Test IVD) using transformer T_D . This allows both the test signal V and the detector input V_D to be grounded.

When the quadrature error component is much larger than the in-phase component, an appropriate quadrature voltage V_Q is injected through transformer T_Q to reduce the quadrature error to a level that can be measured by the detector without compromising the in-phase measurement accuracy. The amplitude of V_Q , which is a function of the ratio of resistors R_1 and R_2 , is used to compute the quadrature error of the Test IVD.

For complete automation, bridge components either span the frequency range or are remotely switched for lowand high-frequency ranges. For example, two sets of isolation and injection transformers $(T_I, T_Q, \text{ and } T_D)$ are needed to cover the frequency range of 10 Hz-100 kHz. These transformers can be selected either manually or remotely. Also, the voltage divider is adjustable in three ranges using different resistors for R_1 and R_2 .

III. ALIGNMENT PROCEDURE

A commercial lock-in amplifier serves as a detector for the bridge. Lock-in amplifiers are able to resolve small in-phase signals in the presence of large quadrature components. However, because of alignment complexities, they are seldom used to their full potential. An alignment procedure (described below) allows the lock-in amplifier to provide direct reading of in-phase and quadrature error components without a precise null balance.

An automatic alignment procedure is performed by phase shifting the reference signal in the detector to find the in-phase and quadrature projections of the voltage difference between the Standard and Test IVD's, $V_s - V_t$, on the Standard IVD output V_s . This procedure consists of the two steps described below.

A. Detector Reference Alignment (See Fig. 2)

The Standard and Test IVD's are set to the nominal test ratio, and the voltage difference between their taps V_{D1} is measured. The Standard divider is then set to 1.001 times the nominal test ratio, and the corresponding difference V_{D2} is measured. We assume that linear step D is in phase with the output of the Standard IVD, and the magnitude of this step can be calculated from measurement data. The

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Fig. 1. Bridge for calibration of both manual and programmable IVD's.



Fig. 2. Vector representation of the detector reference alignment procedure.

lock-in amplifier records the magnitude and phase of the measured signals, and by vector algebra, it is possible to calculate the in-phase P and quadrature Q errors:

$$D^{2} = V_{D1}^{2} + V_{D2}^{2} - 2 V_{D1} V_{D2} \cos \phi$$
(1)

$$\alpha = \cos^{-1} \left(V_{D1}^2 + D^2 - V_{D2}^2 \right) / 2V_{D1} D \qquad (2$$

$$P = V_{D1} \cos \alpha, \text{ and } Q = V_{D1} \sin \alpha.$$
(3)

By performing these two measurements, the detector reference signal can be aligned with the linear step, allowing P and Q to be read directly from the detector display.

B. Quadrature Alignment (See Fig. 3)

The Standard and Test IVD's are set to the nominal test ratio. The phase of the quadrature injection signal V_Q is set to 90° at the appropriate magnitude. The voltage difference V_{D3} is measured. A second measurement V_{D4} is performed after phase shifting the quadrature injection signal by $\Delta \phi_B$. These two measurements provide enough information to compute the correction ξ for the phase angle of the quadrature injection signal.

$$\Delta P = V_{D4} \cos \gamma - V_{D3} \cos \beta \tag{4}$$

$$\Delta Q = V_{D4} \sin \gamma - V_{D3} \sin \beta \tag{5}$$

$$\xi = \arctan\left(\left(\Delta Q/\Delta P\right)\right) - \Delta \phi_B/2.$$
 (6)



Fig. 3. Vector representation of the quadrature injection alignment procedure.

When properly aligned, the detector is able to resolve an in-phase signal that is 40 dB below the quadrature signal, allowing the bridge to be balanced with a single iteration.

IV. BINARY INDUCTIVE VOLTAGE DIVIDER

A 30 b BIVD had been developed to measure the differential linearity of a decade IVD used in a temperature bridge for the Zeno project [10]. For this application, a resolution of one part in 109 was required, and it was felt that a binary divider was a good choice because it offered a structure with a different error pattern than the decade divider. Several BIVD designs were considered, including a technique similar to that described in [8], which combines inductive and resistive dividers to achieve the required resolution. However, we thought that electronic noise from the resistive divider (a multiplying digital-toanalog converter) might cause problems at the low signal levels, so it was decided to construct a relay-switched 30 b BIVD similar to the 20 b BIVD's described briefly in [6] and [8]. The BIVD consists of n center-tapped transformers that can be connected to form 2^n different ratios $(2^{30}$ is approximately 10^9). We later decided to use this 30 b BIVD as a standard in the bridge described above for calibrating programmable IVD's.

Shown schematically in Fig. 4, the BIVD consists of four relay-switched, binary transformers that are con-

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Fig. 4. 30 b BIVD.

trolled via the General Purpose Interface Bus (GPIB). The first section is a two-stage 7 b binary inductive voltage divider designed to operate at low frequencies. It consists of a magnetizing winding and seven separate ratio windings in a binary sequence. The second section consists of 8 b coupled to the first by two-stage techniques. The third and fourth sections are small single-stage binary transformers with 8 and 7 b respectively.

One of the advantages of the binary divider over the conventional decade divider is that it takes only about one third as many switches to achieve the same resolution. A disadvantage is that all of the relays are in series in the signal path, increasing the effective winding resistance. To minimize this influence, relays with less than 0.01 Ω contact resistance and 0.001 Ω repeatability were selected.

Each transformer consists of a twisted pair connected to form a center tap. The winding technique provides excellent symmetry, resulting in a well-defined center tap over a wide frequency range. The disadvantage of the twisted pair is that it produces a large interwinding capacitance. The BIVD is designed to have optimum performance in the low audio frequency range when all four sections are used. As the operating frequency increases, the most significant sections are switched out to maintain maximum accuracy. The sections used (and subsequent resolution) at various frequencies are given in Table I.

A. BIVD Performance Tests

The simplest IVD is a 1 b BIVD, which is simply a center-tapped autotransformer. It is relatively easy to test the symmetry of the center tap by measuring the tap voltage with the input leads in direct and reversed positions [see Fig. 5(a)]. If a second transformer with half the turns of the first is wound on the same core, ratios of 1/4 or 3/4 may be obtained by connecting this winding, as shown in Fig. 5(b). Ideally, this connection should not

TABLE I BIVD RESOLUTION ON DIFFERENT FREQUENCY RANGES

Frequency Range	Sections Used	Total Number of Bits	Resolution (ppm)
10 Hz-2 kHz	1, 2, 3, 4	30	0.001
2 kHz-20 kHz	2, 3, 4	23	0.1
20 kHz-100 kHz	3, 4	15	30

load the first transformer since the voltage developed across the second transformer is approximately the same as the voltage across 1/2 of the first transformer. The extent to which this second transformer degrades the center tap of the first can be measured using the reversing technique, with and without the second transformer connected. A 3 b divider was constructed and characterized using this bootstrap approach.

Uncertainties E_n for the center taps of the first 3 b on the standard divider are given by

$$E_1 = 1/2 \epsilon_1 \tag{7}$$

$$E_2 = E_1 + 1/4 \epsilon_2 \tag{8}$$

$$E_3 = E_2 + 1/8 \epsilon_3$$
 (9)

where

 ϵ_n is the difference between the direct and reversed positions $(V_{Dn} - V_{Rn})/V$,

n is the bit number (the errors are measured with lower bits connected),

 V_{Dn} is the voltage difference between the taps of the BIVD and the standard divider *n* in the direct position,

 V_{Rn} is the voltage difference between the taps of the BIVD and the standard divider *n* in the reversed position, and

V is the voltage applied to both dividers.

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(a)

(b) Fig. 5. (a) Reversing technique. (b) Standard 3 b IVD.

n=3

n=2

The 3 b standard divider was then used as the standard to calibrate the errors of the first 3 b of the programmable 30 b BIVD. The BIVD bit error b_n is given by

$$b_n = (V_{Dn} - V_0) / V \tag{10}$$

where

n=1

 V_{Dn} is the voltage difference between the taps of the standard divider and the BIVD with both set to ratio 2^{-n} , V_0 is the voltage difference between the taps of the standard divider and the BIVD with both set to ratio 0.

Because of the binary structure of this instrument, significant errors are likely to occur at the bit transitions. For example, the binary code for ratio 0.5 is 1000 0000 \cdots , where the most significant bit (MSB) is on and the lower or least significant bits (LSB's) are off. In this condition, the output is connected directly to the center tap of the first transformer. Reducing the ratio by one LSB produces the binary code 0111 1111 \cdots . In this condition, the output is connected through the center taps of all 30 trans-

TABLE II The BIVD BIT Errors and BIT Transition Errors for the First 3 b at 400 Hz

Nominal Ratios	Bit Error Uncertainties	(b_n) and (U_n) in ppm	Bit Transition Errors (e_n) in ppm		
	In-Phase	Quadrature	In-Phase	Quadrature	
0.125	0.04 ± 0.11	0.07 ± 1.00	0.01	0.03	
0.25	0.03 ± 0.06	0.30 ± 1.00	0.03	0.20	
0.5	0.05 ± 0.04	0.70 ± 0.85	0.02	1.50	
0.75 ^a	0.09 ± 0.06	0.60 ± 1.00	0.02	0.30	
0.875 ^a	0.07 ± 0.11	0.60 ± 1.00	0.02	0.60	

^{*a*} These ratios were obtained by setting a single bit and reversing transformer.

			TAF	BLE III							
The BIVD	Віт	ERRORS AND	Віт	TRANSITION	Errors	FOR	THE	MSB			

Frequency (kHz)	Bit Error Uncertaintie	rs (b_1) and rs (U_1) in ppm	Bit Transition Errors (e_1) in ppm		
	In-Phase	Quadrature	In-Phase	Quadrature	
0.010	1.00 ± 0.40	4.50 ± 0.50	0.80	7.00	
0.100	0.10 ± 0.06	0.05 ± 0.10	0.05	0.15	
. 1	0.02 ± 0.04	1.50 ± 0.50	0.30	3.80	
10	1.00 ± 0.11	2.50 ± 1.50	1.30	1.80	
100	2.50 ± 0.90	43.0 ± 6.00	8.00	12.3	

formers. We call the difference between these errors the bit transition error e_n and define it as

$$e_n = (V_{Dn} - V_{LSB} - V_{Ln})/V$$
 (11)

where

 $V_{\rm LSB}$ is the ideal voltage of the least significant bit,

 V_{Ln} is the voltage difference between the taps of the standard divider set to ratio 2^{-n} and the BIVD set to ratio $2^{-n} - 1$ LSB.

Early measurements [11] indicated that the bit transition errors below the third bit contribute no more than one part in 10^8 . Both the bit errors and the bit transition errors of the 30 b BIVD were measured using the 3 b standard divider described above. The total uncertainties U_n represent a combination of the center-tap uncertainties of the standard BIVD E_n and the random uncertainties of the bridge measurements. Results of measurements at 400 Hz, as well as the estimated uncertainties, are summarized in Table II.

Similar test results at other frequencies are given in Table III. For simplicity, only figures for the MSB (nominal ratio 0.5) are provided.

The results in Tables II and III were obtained by comparing the 30 b BIVD to a characterized 3 b standard divider using the bridge described above. The uncertainties are the same for both bit and bit transition errors. The BIVD was also tested at decade ratios. The comparison between binary and decade structures is quite powerful in the way that it exercises many of the BIVD bits, rather than just the most significant bits. Results of the tests made using the standard decade IVD calibration system [12], at AVRAMOV et al .: IVD BRIDGE FOR OPERATION FROM 10 Hz TO 100 kHz

TABLE IV The BIVD Errors Based on the Standard Decade IVD

Nominal Ratio	Frequency: Errors	100 Hz BIVD s in ppm	Frequency: 1 kHz BIVD Errors in ppm		
	In-Phase	Quadrature	In-Phase	Quadrature	
0.1	0.01	0.09	0.05	0.72	
0.2	0.01	0.34	0.09	2.06	
0.3	0.02	0.79	0.15	3.70	
0.4	0.00	0.28	0.19	5.25	
0.5	0.02	0.30	0.03	2.58	
0.6	0.03	0.29	0.02	3.87	
0.7	0.01	0.76	0.04	5.88	
0.8	0.04	0.46	0.23	2.72	
0.9	0.02	0.29	0.18	4.90	

100 Hz and 1 kHz, are given in Table IV. Measurement uncertainties were ± 0.5 ppm for the in-phase and ± 5 ppm for the quadrature components. The results of measurements made using these two systems agree to within their combined uncertainties.

V. CONCLUSIONS

A bridge for calibrating programmable IVD's has been described. A procedure to align the bridge detector was developed to simplify balancing by providing direct reading of the in-phase and quadrature error components. A 30 b BIVD, which operates from 10 Hz to 100 kHz, serves as the standard for the new bridge. Once the alignment procedures have been completed, automatic measurements can normally be performed in less than 1 min/test point. In general, the accuracy of measurements made using this bridge is comparable to those made using the best manual IVD standards.

Since complete characterization of the BIVD errors is laborious, future work will include an analysis of the bit and bit transition errors to reduce complexity and possibly enhance accuracy. Also, further study is needed to characterize the bridge at higher frequencies where ratio uncertainties are expected to be on the order $\pm 0.3F$ ppm out to 100 kHz, where F is the test frequency in kilohertz.

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