IGBT Model Validation

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Half-bridge transistor topologies, and their related full-bridge and three-phase counterparts, are very common in power conversion applications because they can deliver push-pull power to the load with a minimum of voltage-stress to the transistors. In order to optimize the switching operation of a transistor pair configured as a half-bridge, one needs to pay particular attention to the gate-drive circuit impedance characteristics and timing. The details of the transition interval, when one device turns off and the other turns on, have a large influence on circuit efficiency and reliability.

The Insulated Gate Bipolar Transistor (IGBT) is becoming the power switch of choice for many power applications because it offers a good compromise between on-state losses, switching speed and losses, and ease of use. The IGBT has enjoyed particularly deep penetration in the field of motion control where supply bus voltages range from 300 V to several times higher. To accommodate these voltages, a large variety of IGBTs are available today with a 600 V to 1200 V blocking capability. Devices with higher voltage ratings are also being made by various manufacturers. IGBTs are now offered both as single devices or packaged in modules with multiple IGBTs and/or diodes. Some modules include driver circuitry as well.

In recent years, efforts to model the switching behavior of IGBTs have been greatly expanded [1]-[6]. In many cases, circuit modeling has become an economic necessity because the cost of the components of a medium- to high-power circuit, and the load itself, is so high that all means available must be used to lower the risk of system failure during both the prototyping phase of product development and production.

As the physics that govern transistor behavior are quite complex, attempts at accurately predicting the details of transistor switching performance tax models to their extreme. Test procedures are needed to check the validity of predictions made by various models, and these procedures need to be applicable to commonly used circuits. It is particularly important that these test procedures are built around a testbed that is well understood and well characterized so that the device model is given the correct information for the simulations. The details of a suitable testbed circuit that can be used for model-verification-related measurements on half-bridge configured IGBTs are given here.

The NIST/IEEE Working Group on Model Validation [7] has been established to address the need for testing the validity of various models as they relate to predicting the behavior of devices under realistic conditions. The work described in this article is performed, in part, to support the needs of the IGBT task of the Working Group.

Test Circuit Description

Fig. 1(a) shows a block diagram of the test circuit, along with the IGBTs and their drive and load components. The IGBTs are configured in a half-bridge which drives a load-resistor through a dc blocking capacitor. A dc voltage supply is connected across the half-bridge in a conventional manner. Bypass capacitors for the supply are present, but not shown. A resistive load was used for the work described in this article because an inductive load would generally require commutation di-

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odes that would likely complicate the model verification process. IGBTs Q1 and Q2 are identical types for the present work, although nonidentical types could be used. Gate impedances Z1 and Z2 can be independently changed to achieve a range of switching speeds. All measurements shown in this work are taken with respect to the low-side switch Q1.

The elements on the left-hand side of Fig. 1(a) determine the timing of switching events in the circuit, and Fig. 1(b) shows a portion of the timing waveforms for the IGBT gate drives during the time period when the gated H-bridge drivers are active. The square-wave generator of Fig. 1(a) provides a 17 kHz square wave that is applied to each of the gated H-bridge drives for the IGBTs. A variable delay line is inserted in line between the generator and the drive for the high-side switch. Each IGBT is driven through a gate drive transformer coupled from an H-bridge configuration of power MOSFETs. The 17 kHz generator also drives a gating counter. The counter causes operating power to be applied to the two H-bridge drives in a manner such that only bursts of eight cycles every 120 ms are actually applied to the IGBT gates. This low effective testing duty cycle greatly reduces heat-sinking requirements for the IGBTs, but still provides multiple-cycle operation so as to simulate realistic switching conditions.

Transformer coupling to the gates of the IGBTs was chosen over direct coupling primarily for reasons of robustness and isolation. The transformer coupling from the H-bridge drive described in this work prevents the gate drive circuits from being destroyed in the event of IGBT failure. The transformers also provide ground isolation and high-quality high-side drive isolation, which improve the quality of the measured waveforms. The main problem with the transformers is that they are difficult to make. The leakage inductance is a critical parameter that must be minimized in order to make them able to deliver high-gate current quickly, with a minimum of ringing. Details of transformer construction, as well as the complete circuit, are given in the appendix.

Test Circuit Operation

Examples of typical measured waveforms obtained from the circuit described above are given in this section of the article. The first case described is re-

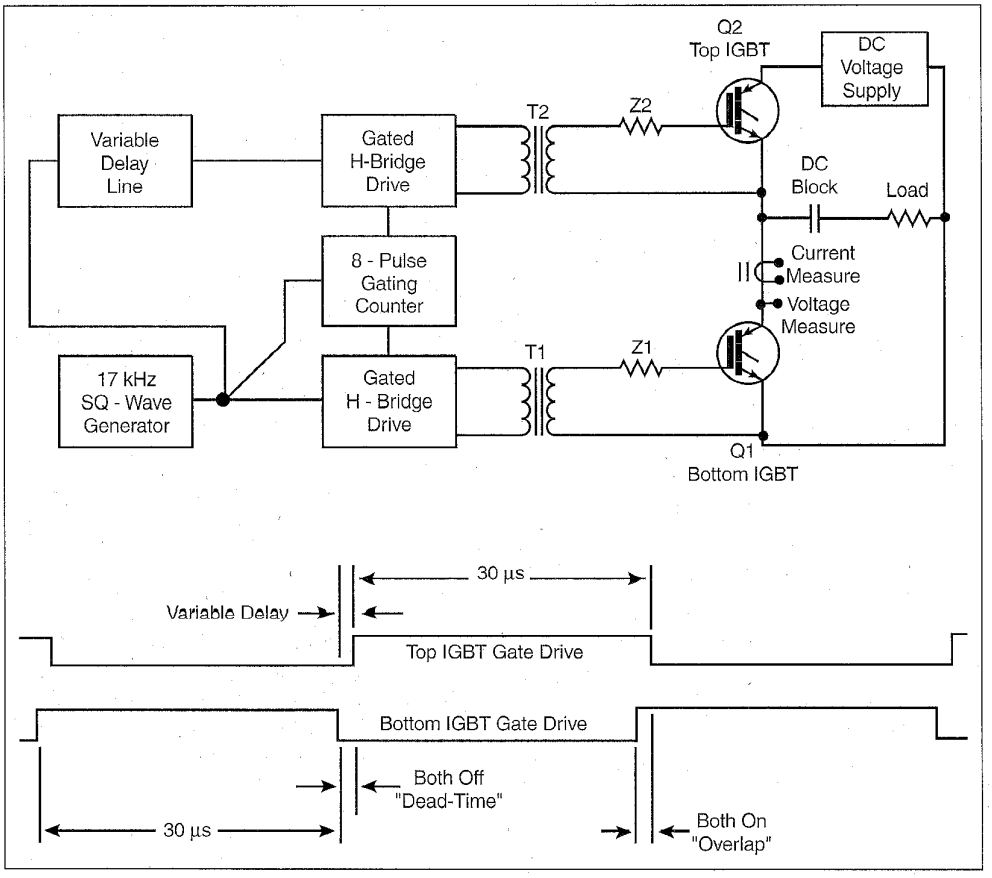

Fig. 1. Shoot-through testbed showing (a) block diagram indicating IGBTs and their associated components and (b) gate-drive timing showing the delay with dead-time and overlap intervals.

ferred to as "dead-time," and applies to the time interval when both IGBTs are off as indicated in Fig. 1(b). In this case, the low-side switch Q1 is initially on and conducting load-current while the high-side switch Q2 is off. At the end of the 30 μs pulse, determined by the 17 kHz square-wave generator, Q1 is turned off. After a delay interval which can be adjusted, Q2 is turned on so that load-current is resumed, but in the opposite direction. This particular case represents desirable transition of current between devices in the half-bridge IGBT pair [8]. In this article, the term "dead-time" is used to describe the time interval between when the low-side switch is turned off and the high-side switch is turned on.

Details of transformer construction, as well as the complete circuit, are given in the appendix.

The second case described is referred to as "overlap" and applies to the time interval when both IGBTs are on, as indicated in Fig. 1(b). In this case, the high-side switch Q2 is initially on and supplying load current while the low-side switch Q1 is off. At the beginning of the overlap interval, Q1 is turned on and Q2 remains turned on until the adjustable delay period expires. After the delay period, Q2 is turned off, while Q1 continues to conduct the load-current.

The overlap case represents a shoot-through condition characterized by rapidly increasing current passing through both IGBTs and bypassing the load. In the event that the time interval between when the low-side switch is turned on and the high-side switch is turned off is too long, the IGBTs will be destroyed. This case represents undesirable half-bridge IGBT operation and could be caused by improper gate drive design or system faults. In this article, the term "overlap" is used to describe the time interval between when the low-side switch is turned on and the high-side switch is turned off.

The overlap case can also be used to emulate the stress that an IGBT experiences during turn-on with the reverse recovery of a diode [8]. Many circuits contain inductive loads with commutating diodes, whereby an IGBT turns on and is subjected to a similar type of short circuit during the time in which the diode is undergoing reverse recovery. In the diode emulation discussion below, choices of gate drive resistors and delay are demonstrated to determine some commonly specified diode parameters. This diode emulation feature provides additional uses for this circuit in verifying IGBT models.

Dead-Time Case Description

Referring again to Fig. 1(a), all waveform measurements are taken with respect to the low-side switch Q1 as shown. The common ground is the emitter terminal of Q1, and both collector- and gate-voltage are measured with respect to this ground. Fig. 2 shows the a) collector-voltage, b) collector-current, c) gate-voltage and gate-drive voltage applied to the gate resistor, and d) gate-current for a delay setting of 80 ns. IGBTs Q1 and Q2 are ultra-fast buffer-layer types, gate impedances Z1 and Z2 are 62 Ω resistors, the load-resistance is 30 Ω, and the supply-voltage is 300 V. (In this article, the terms "collector" and "emitter" are used to refer to the external terminals of the IGBT in accordance with the proposed JEDEC standards [9]. Discussions that relate to the internal operation of the IGBT use the terms internal collector or internal emitter, which are not the same as the external terminals named by the proposed standard.)

Fig. 2(a) shows the collector-voltage rising, first from the on-state voltage of Q1 as Q1 turns off, to a mid-point voltage of around 150 V, and then towards the supply-voltage of 300 V when Q2 turns on after the delay. The collector-voltage does not

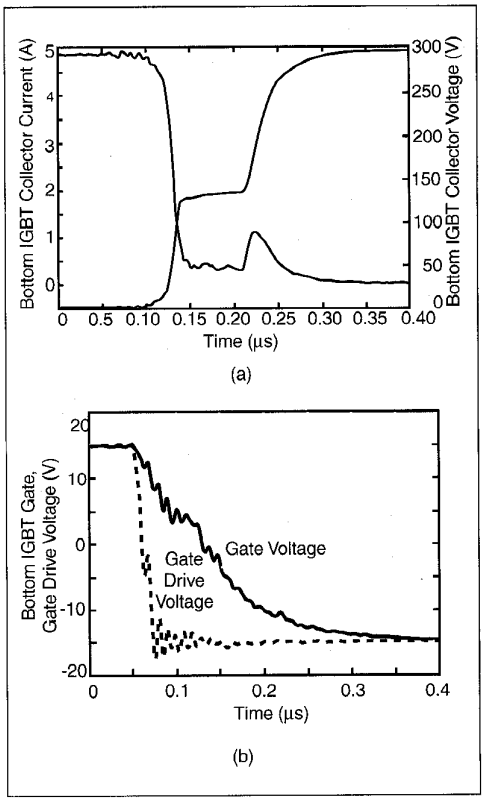

Fig. 2. Switching waveforms for dead-time interval showing (a) collector-voltage; (b) collector-current; (c) gate-voltage and drive voltage applied to gate resistor, and (d) gate-current.

fully reach the blocking capacitor voltage of 150 V at the first plateau, because the tail-current in Q1 results in a voltage drop across the load-resistor. It should be noted that the delay time, while predominantly determined by the delay switch-box in the circuit, is also influenced by the gate-drive impedances Z1 and Z2.

Fig. 2(b) shows the collector current of Q1 for the turn-off. The collector-current is initially equal to the load-current. When the gate-voltage is switched below threshold, the collector current drops rapidly from nearly 5 A to about 0.5 A during the time that the voltage rises towards 150 V. During the dead-time interval, that is, before Q2 is switched on, a current-tail exists in Q1, which is due to the slowly decaying excess internal carrier base charge present in the IGBT. As the collector-voltage is driven towards 300 V by the turn-on of Q2, the current-tail in Q1 shows a bump.

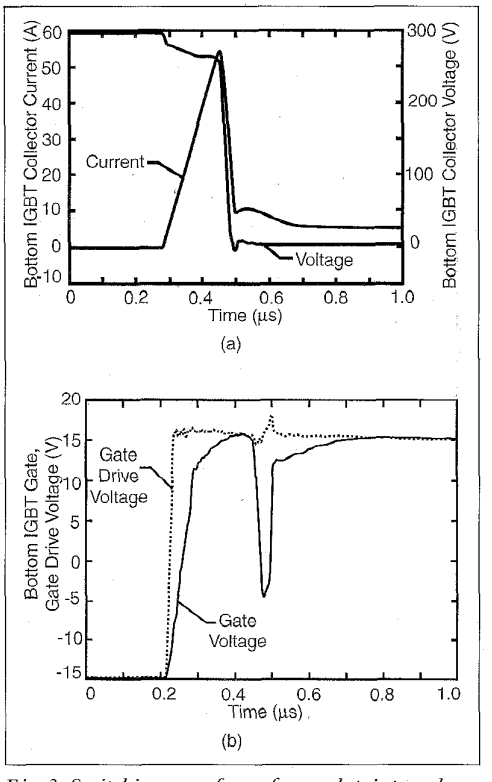

Fig. 3. Switching waveforms for overlap interval showing (a) collector-voltage; (b) collector-current; (c) gate-voltage and drive voltage applied to gate resistor, and (d) gate-current.

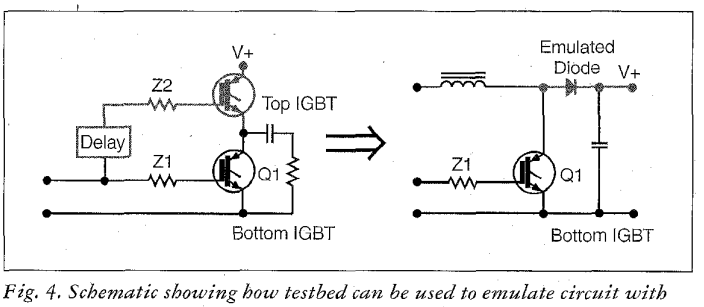

Fig. 4. Schematic showing how testbed can be used to emulate circuit with IGBT turn-on and diode reverse-recovery. The delay and the value of Z2 can be independently varied to emulate various diode characteristics.

The tail-current bump is caused by a decrease in the neutral-base width in the IGBT, which, in turn, increases the internal collector-current for a given base charge [1], [10]. The current bump rise time is affected by the voltage rise time, which in turn, is affected by the choice of the gate-resistor used for Q2. The tail-current bump decay time is determined by the IGBT effective lifetime. For buffer layer IGBTs, this lifetime is much smaller at 300 V than it is at 150 V, and the current bump decay rate is faster than the decay rate before the bump [1].

Shoot-Through Case Description

Fig. 3 shows the a) collector-voltage, b) collector-current, c) gate-voltage and gate-drive voltage applied to the gate-resistor, and d) gate-current for an overlap setting of 200 ns. The other circuit parameters remain the same as for the dead-time case discussed above. Immediately upon Q1 turning on, a rather constant *di/dt* of about 333 A/μs occurs. The rate of collector-current rise during the overlap interval is determined primarily by the feedback voltage developed across the emitter lead inductance of Q1, the gate resistor value, the drive-voltage applied to the gate resistor, and the gate-charging characteristics of the IGBT.

As a result of the constant *di/dt*, there is initially a 20 V drop in the measured-collector voltage caused by series inductance. The inductance is due to the collector and emitter leads of Q2, which are approximately 9 nH each [11] and the power supply inductance, which is about 38 nH. The series inductance between the power supply and Q1 is, therefore, approximately 56 nH. The methodology used to determine testbed parasitics is described in the model validation section of this article. This measured value of series inductance is consistent with a 60 nH inductance estimated by considering the 333 A/μs *di/dt* and the 20 V drop observed in the figure.

After the initial drop of 20 V on the collector, the voltage continues to fall slowly, and then begins to level out after about 100 ns. This behavior is due to the dynamic conductivity-modulation of Q2 in response to the increasing current demand during the overlap interval.

Once the overlap time period expires, Q2 is switched off while Q1 remains on. The collector current of Q1 then falls to the load-current of 5 A and the collector-voltage falls towards the on-state voltage. The current initially has a rather constant rate of fall, followed by the classic IGBT current

The test circuit for the overlap condition can also be used to subject the IGBT to conditions that it would experience during normal operation in application circuits that include an inductor and a commutating diode.

tail from Q2. The rate of current fall once the turn-off of Q2 commences is determined primarily by the feedback voltage developed across the emitter lead inductance of Q2, the gate resistor value, the applied turn-off gate-drive voltage, and the gate-charging characteristics of the IGBT, until the tail-current begins to dominate. These current waveforms are discussed further in the section on diode emulation.

Diode Emulation

The test circuit for the overlap condition can also be used to subject the IGBT being tested, Q1, to conditions that it would experience during normal operation in application circuits that include an inductor and a commutating diode. Such an application circuit may not even be a half-bridge, but may include only a low-side switch. An example of such a circuit is the boost-converter commonly used for power factor correction. Fig. 4 is a schematic indicating that the test circuit on the left-hand side of the figure can be used to emulate the conditions of diode recovery of the circuit on the right-hand side. The diode characteristics to be emulated are determined by Q2, Z2, and the delay.

The primary advantage in using a second IGBT to emulate a diode instead of an actual diode is that only one semiconductor model is being tested during the circuit simulation. A second advantage of using the second IGBT is that the emulated diode parameters are easy to change so that the IGBT model can be evaluated for the full range of possible diode characteristics.

In Fig. 5, the overlap time is varied to emulate the effects that the IGBT would experience during the recovery of various diodes with different stored-charge characteristics. For this set of curves, both of the gate resistors in the shoot-through test circuit are 62 Ω. Several features of the waveforms associated with emulated diode recovery are indicated in the figure.

Initially (before Q1 is switched on), the emulated diode conducts the full 5 A load current. When Q1 is switched on, it is forced to carry the load-current plus the reverse-recovery current of the emulated diode. For the curve with the longest overlap, the emulated peak reverse-recovery current is about 50 A, resulting in a peak IGBT current of 55 A. The tail current at the end of the emulated diode recovery is due to Q2 and may have a different shape than the diode being emulated. It is, therefore, recommended that a fast IGBT with a small tail be used for Q2 and that if other diode tail shapes are desired, they could be emulated with additional circuit complexity.

The values of the gate resistors can be changed to tailor the shape of the emulated diode recovery. In characterizing diodes, it is common practice to divide the recovery current into a t_a portion and a t_b portion. The t_a portion is the time from when the diode current passes through zero as it moves from forward-current conduction into the recovery phase, and the time when the reverse current reaches its maximum value. The t_b portion begins with the termination of t_a and ends when the current has fallen to some logical termination point such as 10 percent of maximum. (Sometimes the termination of t_b is defined differently, as there are a wide range of shapes of current waveforms at the end of the recovery for different diodes.)

Fig. 6 shows collector-current waveforms with three different sets of emulated diode recovery characteristics indicating the t_a and t_b periods. These current waveforms were made using three different Q2 gate resistors having values of 240 Ω, 62 Ω, and 16 Ω to affect the *di/dt* during the emulated t_b portion of diode recovery. The value of the gate resistor for Q1 was 62 Ω for all three curves so the di/dt during the t_a portion remains unchanged. This test can be used to emulate diodes with different snappiness characteristics (defined as the ratio of t_a to t_b). To make the relative slope differences more evident, the overlap time intervals were also adjusted to make the currents cross one another during a given point during the t_b period.

Fig. 7 shows how changing the gate-resistor on Q1 changes the di/dt of the emulated diode recovery during the t_a period, but leaves the di/dt during

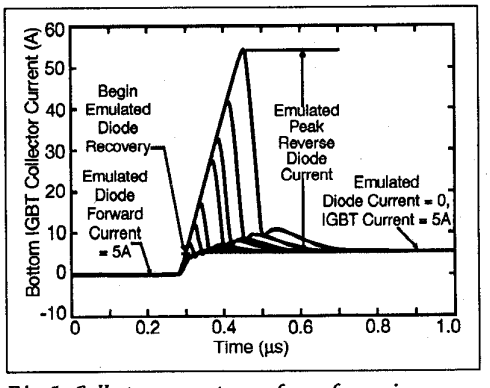

Fig. 5. Collector-current waveforms for various overlap intervals emulating IGBT turn-on recovering various diodes with different quantities of recovered charge.

the t_b period unchanged. To make the relative slope differences more evident, the overlap time intervals were also adjusted to make the currents peak at the same value. It should be noted that as the overlap was increased with increasing gate resistance, the curves corresponded to diodes with larger emulated recovered charge. One could also produce curves with equal values of recovered charge by choosing suitable overlap times.

Model Validation Procedure

Various physics-based IGBT models are presently provided within commercial circuit simulation programs. For example, Saber 4.0 [4] provides both the buffer-layer [1] and nonbuffer-layer [3] IGBT models developed by Hefner as well as an electro-thermal version of each model [2]. Recently, PSPICE 6.3 [6] also includes the nonbuffer-layer IGBT model developed by Hefner [5].

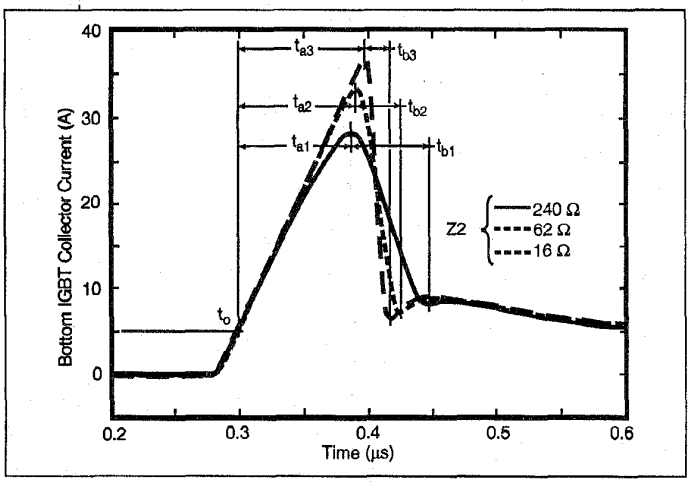

Fig. 6. Collector-current waveforms for overlap intervals emulating IGBT turn-on recovering diodes with different degrees of snappiness.

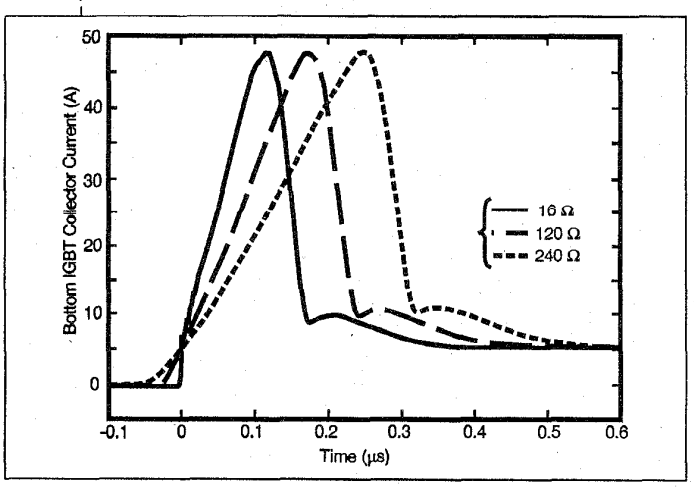

Fig. 7. Collector-current waveforms for overlap intervals emulating IGBT turn-on recovering diodes at various di/dt rates.

In this section, a brief example is given on how the measurements made with the shoot-through testbed can be applied to model validation.

(Saber is a trademark of Analogy, Inc., Beaverton, Oregon. PSPICE is a trademark of MicroSim, Inc., Irvine, California.) In addition to the different model versions and simulator implementations, different laboratories with different equipment and experience extract the model parameter sets. Therefore, it is essential to have well-established validation procedures that can be used to independently validate each of the models provided in different simulators for different IGBT manufacturer part numbers.

The IGBT task of the NIST/IEEE Working Group on Model Validation is currently in the process of establishing the "IEEE Recommended Practice for Test Procedures for IGBT Circuit Simulator Model Validation." The IGBT shoot-through test is proposed, herewith, for consideration as one of the recommended test procedures. In this section, a brief example is given on how the measurements made with the shoot-through testbed described in the last section can be applied to model validation. The device and circuit characterization necessary to assure correspondence between the conditions that are simulated and measured are also described. Finally, recommendations are given on selecting the ranges of test circuit parameters for which a given model should be validated.

Test Circuit Characterization

Fig. 8 shows the schematic of the testbed used for the simulations with the parasitic circuit elements included. The voltage nodes and the measured values of the parasitic elements are indicated on the figure. Parasitic elements are included to represent the power supply inductance LSUP, gate-drive circuit inductances LDH and LDL, and the effective common-mode inductance LCM and capacitance CCM. The other parasitic inductances shown include 9 nH estimated lead inductances for each lead of the TO-220 packaged IGBTs.

The gate resistors RGH and RGL are varied in the simulations in accordance with the values used in obtaining the experimental waveforms. The load resistor RL and dc blocking capacitor CB have values of 30 Ω and 50 μF, respectively, in all simulations, and in all experiments.

The gate-drive generators are characterized as having very low-source resistance by virtue of their H-bridge MOSFET drive, but limited in current by the inductance of the gate-drive transformers.

The effective inductance was determined to be 90 nH, which was measured by observing *di/dt* in a 2 Ω non-inductive resistor soldered across the gate-drive transformer output with lead length equivalent to the gate-emitter drive loop minus the IGBT lead lengths. Most of the 90 nH is leakage inductance in the transformer.

The basic risetime of the gate-drive unloaded is 20 ns. The primary of the gate-drive transformer also showed a 20 ns risetime. The risetime on the primary showed negligible change when the 2 Ω load was connected across the secondary, but the risetime on the secondary slowed to about 200 ns, confirming the purely inductive nature of the gate-drive generator. Therefore, the gate-drive generators are modeled as an inductor in series with an ideal pulse generator having linear rise and fall transitions of 20 ns, separated by 30 µs constant gate-voltage segments.

The gate drive transformers have a primary-to-secondary capacitance of 370 pF, as discussed in the Appendix. This is of little consequence for the low-side switch driver transformer because both primary and secondary are near ground potential. The matter is more serious for the high-side switch driver transformer because its secondary must follow the large *dv/dt* appearing at the V out terminal. If this capacitance were allowed to couple the output *dv/dt* to ground through the transformer there would be a significant error in the current measurements as well as increased noise on the measured waveforms.

A common-mode transformer was added in line with the primary of this gate-drive transformer to greatly reduce the peak amplitude of the common-mode current that would otherwise couple through the capacitance in the transformer. The common-mode transformer was added in the primary circuit rather than in the secondary circuit because it adds negligible differential inductance on the primary due to the voltage step-down in the transformer. The common-mode inductance LCM is 620 µH, and this element, along with the common-mode capacitance CCM of 370 pF, is shown in Fig. 8.

The power supply inductance was estimated by duplicating the geometry of the test circuit with an identical type of power supply bypass capacitor soldered to a piece of circuit board that was all copper covered except for a break in the copper that extended across its width. A 5 MHz sine wave of known current amplitude was injected across the break, causing the current to pass around this test loop made up of the circuit board and the bypass capacitor. The inductive reactance of the test loop was measured to be 1.18 Ω, or 38 nH at 5 MHz.

Device Characterization

In addition to characterizing the testbed, the device model being validated must be specified correctly in the simulator. For pre-characterized device models provided in a software vendor's component library, this amounts to simply selecting the manufacturer's part number from the library and possibly specifying parameters required by the model to represent statistical device variations. In the absence of a pre-characterized device model, the simulator should include a well-documented model parameter extraction se-

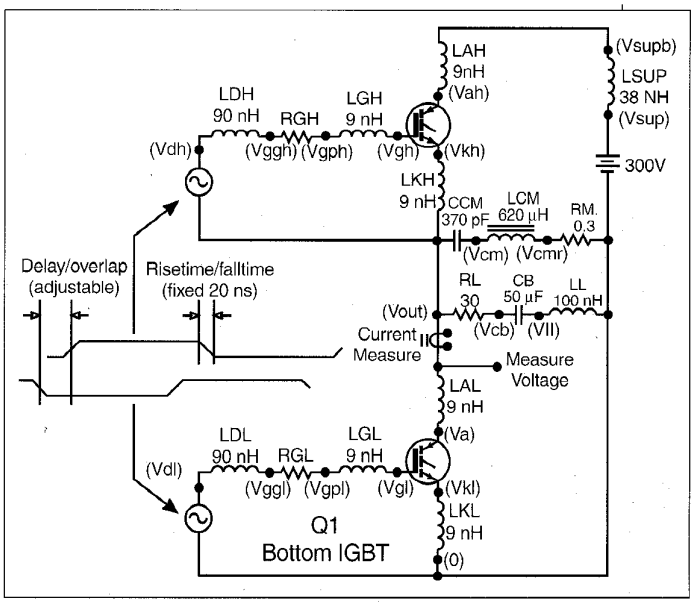

Fig. 8. Schematic of testbed used for model simulation. Node voltages are defined and testbed parasitics are included.

Table 1. Buffer Layer IGBT Model Parameters (300 K)

N_L	1.5×10^{14} cm^{-3}
N_H	2.4×10^{17} cm^{-3}
W_L	60 m
W_H	7 m
L	0.14 s
H	0.03 s
I'_{sne}	2.5×10^{-14} A
A	0.068 cm^2
K_p	2.0 A/V^2
K_f	1.5
V_T	5.0 V
V_{Td}	-5.0 V
A_{gd}	0.034 cm^2
C_{oxd}	0.68 nF
C_{gs}	0.61 nF

quence. Device parameter extraction is used for this article because component libraries are not fully developed for IGBTs. Circuit simulator providers are working to build those libraries.

The device used for the measurements and simulations in this article is an ultra-fast class IGBT that uses a buffer-layer to optimize the trade-off between switching speed and on-state voltage [12], so the buffer-layer IGBT model available in Saber 4.0 [1], [4] provides the most appropriate physical equations for the device. The non-buffer layer IGBT model [3]-[6] would be more appropriate for the so-called "non-punch through" device types and other device types that do not exhibit increased tail decay rate at high voltages [1].

Some of the conditions studied in this article produced current densities in excess of 1000 A/cm^2, which is near the limit of the highest-pulsed current-density rating of presently available IGBTs. Typical continuous current ratings of present-day IGBTs are on the order of 100 A/cm^2. The high-current second-order effects [1] of carrier-carrier scattering and space-charge limited carrier velocity were not included in the simulations in this article so that the model will correspond to that currently available in Saber 4.0. These high-current second-order effects were not included in the original release of the model in Saber 4.0 because the added complexity causes a performance penalty that exceeds the accuracy benefit.

The device used for the measurements and simulations in this article was made using the same IGBT technology as the device described in [1] except that it has twice the active area. The IGBT model parameters were extracted as described in [1] and are listed in Table 1. As expected, by comparing the device parameters listed in the table of this work to those listed in table II of [1], it can be seen that the parameters I_{sne}, A_{gd}, C_{oxd}, C_{gs}, and K_p scale proportional to the device active area A. The other parameters remain relatively unchanged within statistical device-to-device variation.

Sample Comparison of Measured and Simulated Results

Comparisons between measured and simulated dead-time and overlap waveforms were made for a variety of combinations of gate resistors and delay times. The IGBT model parameters listed in the table and the circuit values shown in Fig. 8 were used for the simulations. A Saber net-list was used to implement the circuit of Fig. 8; alternatively, a schematic capture program could have been used. A Saber command script was used to execute the

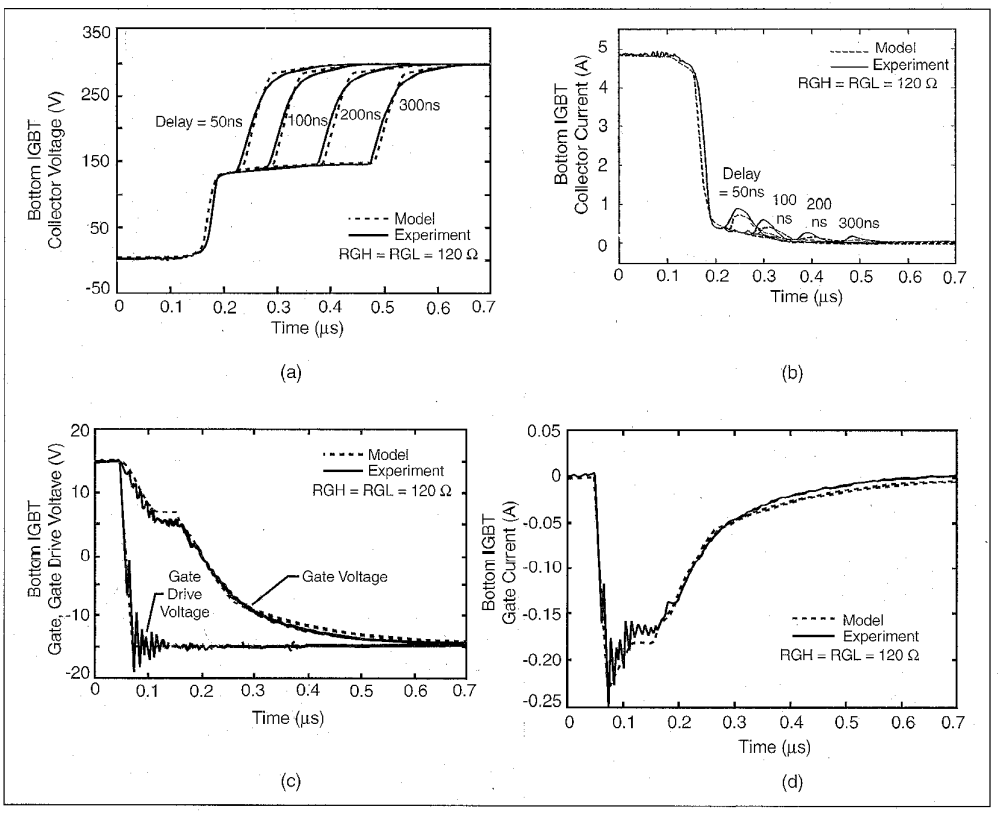

Fig. 9. Comparison of measured and simulated waveforms for dead-time case with several different delays showing (a) collector-voltage; (b) collector-current; (c) gate-voltage and drive voltage applied to gate resistor; and (d) gate-current.

simulations so that multiple combinations of Z1, Z2, and delay times could be specified with a single input file. This approach simplified the simulation and comparison of the many waveforms studied for different values of Z1, Z2, and delay times by reducing the amount of interaction with the program that would otherwise be required.

Fig. 9 shows both the simulated and the measured waveforms for the dead-time case, and Fig. 10 shows those for the overlap case. For these results, both Z1 and Z2 are 120 Ω, and several different delays are pictured. Although results are shown for only one set of gate resistors, the simulations performed similarly for other combinations of gate resistor values. For both experiment and simulation, gate resistor values ranged between 16 Ω and 240 Ω. Both the measured and simulated waveforms exhibit the same features and variation as the values of Z1, Z2, and delay were changed.

The agreement between simulations and measurements of Fig. 9 demonstrates the ability of the IGBT model to describe conditions where voltage is applied to the IGBT collector by external circuit conditions some time after the IGBT has been switched off. This is also important for a variety of soft switching circuit topologies where a tail-current bump occurs as voltage is applied to the IGBT.

The agreement between simulations and measurements of Fig. 10 demonstrates the ability of the IGBT model to describe the fault current that occurs for shoot-through conditions. The ability to describe these waveforms is essential if the IGBT model were to be used to design a fault current detection and shutdown circuit. The agreement of Fig. 10 also demonstrates that the IGBT model is capable of describing the current spike that occurs for turn-on with the reverse recovery of a diode, provided that a similarly validated diode model is available.

Test-Circuit Parameter Selection

For model validation test procedures to be generally applicable, they must include specifications of how the test-circuit parameters are to be chosen, how many measurements should be made, and how the results should be interpreted. The test-circuit parameters should generally be specified in terms of the intended range of operation of each device part number listed in manufacturer's data sheets, circuit application determined values, or in terms of measured features of the device waveforms. In general, it is recommended that comparisons be made for a range of conditions because some of the waveform features may not be noticeable for a single set of test circuit parameters. Inasmuch as this is the first study of the shoot-through model validation test, general specifications on circuit parameter selections cannot be completed here, but the fol-

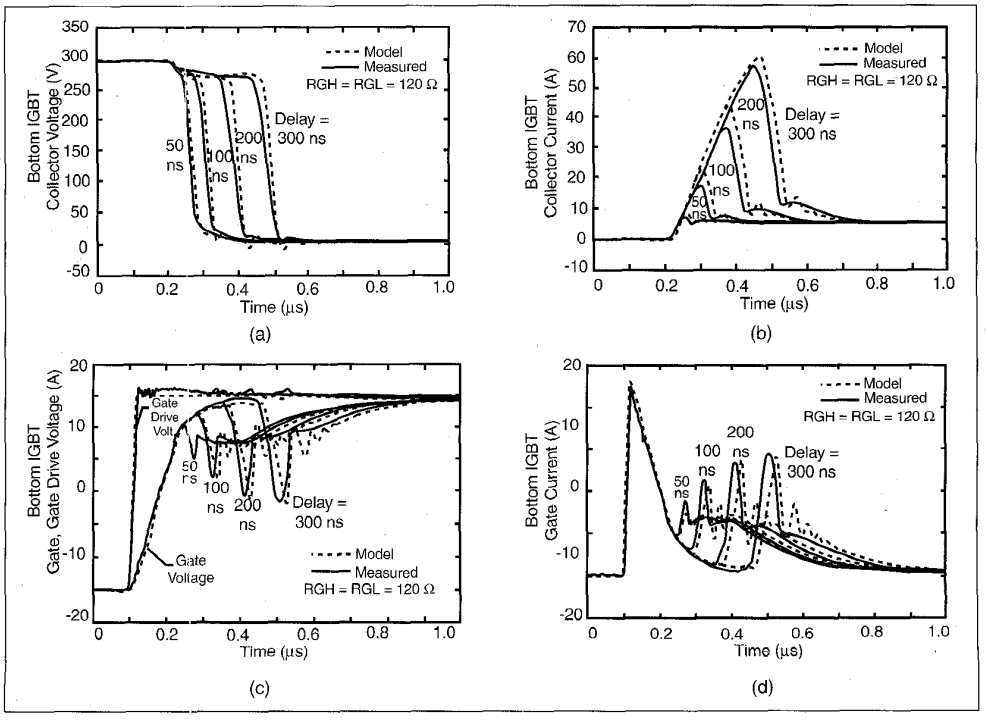

Fig. 10. Comparison of measured and simulated waveforms for overlap case with several different delays showing (a) collector-voltage; (b) collector-current; (c) gate-voltage and drive voltage applied to gate resistor; and (d) gate-current.

lowing discussion describes some of the issues that should be considered.

Gate-resistor values required for the circuit should generally scale inversely with current rating of the device. When considering diode reverse recovery emulation, values of the gate resistors can be chosen so that the effects produced are similar to likely real diode recovery conditions. For example, the gate resistor of the low-side switch should be chosen so that a *di/dt* is produced during the t_a portion, of the diode emulation that is consistent with the manufacturer's specified values of IGBT switching speed and current rating. The gate resistor of the high-side switch can then be chosen to produce an appropriate range of diode snappiness, t_a/t_b. Overlap time intervals can be selected so that the maximum peak-current rating of the device can be approached in order to check the accuracy of the model at the highest-current densities.

It should be noted that gate-drive voltage strongly influences the rate of current rise and fall in the shoot-through test. For most IGBT applications, the positive gate voltage pulse amplitude is around 15 V regardless of device current rating (an exception is ignition IGBTs that are intended to operate at a lower gate-drive voltage). Some application circuits drive the gate both positive and negative, while others limit the off gate voltage to not going negative. It may be desirable to perform the shoot-through test for several gate drive amplitudes to explore the sensitivity of the IGBT current rise and fall to gate drive voltage. Because the tail current and inter-electrode capacitance of IGBT are voltage dependent, it may be advisable to perform the shoot-through tests at several supply voltages.

Conclusion

A circuit has been introduced that enables a variety of measurements to be made on half-bridge IGBT pairs involving the transition of current from one device to the other. The gates of the two IGBTs that form the half-bridge are driven with opposite-polarity square-waves that can be shifted with respect to one another by a variable delay. This delay causes both a "dead-time" interval when both IGBT gates are simultaneously off during the transition of current between the two devices and also an "overlap" interval when both IGBT gates are simultaneously on during the transition of current between devices.

The dead-time interval is characteristic of normal transition of current between the high-side and low-side IGBTs in the half-bridge IGBT transistor pair. When the low-side IGBT is turned off at the beginning of the dead-time interval, the collector-voltage of this IGBT rises toward a mid-voltage point, which is half of the supply voltage. This half-step in the collector voltage is a result of the particular load configuration used in this work. When the high-side IGBT is turned on after the delay, the collector voltage of the low-side switch is driven to the full power supply voltage and a bump occurs in the low-side IGBT current tail. Model validation using the dead-time condition is important for applications where a rise of collector voltage is imposed by external circuit conditions during IGBT turn-off.

The overlap interval is characteristic of a shoot-through condition that could be caused by improper gate drive design or system faults. This condition results in a rapidly increasing shoot-through current passing through both IGBTs and bypassing the load. In the shoot-through testbed described in this article, the peak value of the current can be controlled by adjusting the delay. In addition, the rate of current rise can be adjusted by changing the gate resistor of the low-side IGBT switch, and the rate of current fall at the end of the overlap interval can be adjusted by changing the gate resistor for the high-side switch. Model validation using the overlap condition is important for the design of fault current detection and shutdown circuits. The overlap condition can also be used to validate the IGBT model for conditions of turn-on with the reverse recovery of a diode, where the gate resistor values and overlap time can be used to emulate various diode stored charge and snappiness characteristics.

Suggested procedures are given that enable one to use the shoot-through testbed described in this work for IGBT model validation. A suitable circuit schematic for representing the testbed in a circuit simulator is given that includes the various parasitic elements of the testbed, and methods to extract values of the parasitic elements are described. The selection of test circuit parameters based upon device data sheet information is discussed, and sample comparisons are made between the measured waveforms obtained with the shoot-through testbed and the buffer-layer IGBT model that is provided with Saber 4.0. The model validation procedures described in this article can be applied to the various IGBT models provided for different manufacturer's parts numbers in different commercial circuit simulators.

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Appendix: Detailed Circuit Description

Fig. A1 is a schematic diagram of the driver circuit for the IGBT shoot-through testbed. A 74121 monostable multivibrator (U1) is configured as a 34 kHz oscillator, and its output is fed to a 7493 counter (U2). The first stage of this counter generates a 17 kHz square wave, which becomes the fundamental test waveform for the testbed. The remaining counter stages of U2, and the counter stages of U3 and U4, are used to generate an enabling signal which restricts the testing of the IGBTs to low duty cycles so that heat-sinking requirements are greatly reduced. The enabling signal is generated by a 7430 NAND gate (U5), and causes the IGBT drive to be active for one part in 256. Since the four least significant bits of the composite counter are not applied to the NAND gate, the IGBTs receive a burst of eight switching cycles when the IGBT drive is active.

Transistors Q1-Q5 amplify the 17 kHz square-wave from U2 so that a 50 Ω delay line can be driven with a large signal voltage so that switching noise generated by power switching of the IGBTs will be less likely to perturb the timing of the signals. Two nearly identical gate drive amplifier circuits are shown in Fig. A1; one receives its non-delayed signal directly from the Q4-Q5 buffer, and the other takes its signal from the end of the delay line which is terminated by R22. The delay line is inserted between J1 and J2. The delay can be a length of 50 Ω cable or a passive delay switch-box. Some video delay switch-boxes operate at 75 Ω and R22 can be changed to 75 Ω to optimize this circuit for such a delay line.

Each one of the gate-drive amplifiers consists of two sections. The first section drives a transformer, which in turn drives an H-bridge configured second section. This second section drives the IGBT gate drive transformer. The second section for both of the IGBT drives receives power only during the enabling portion of a complete test cycle, as determined by the entire count of the counter circuitry described earlier.

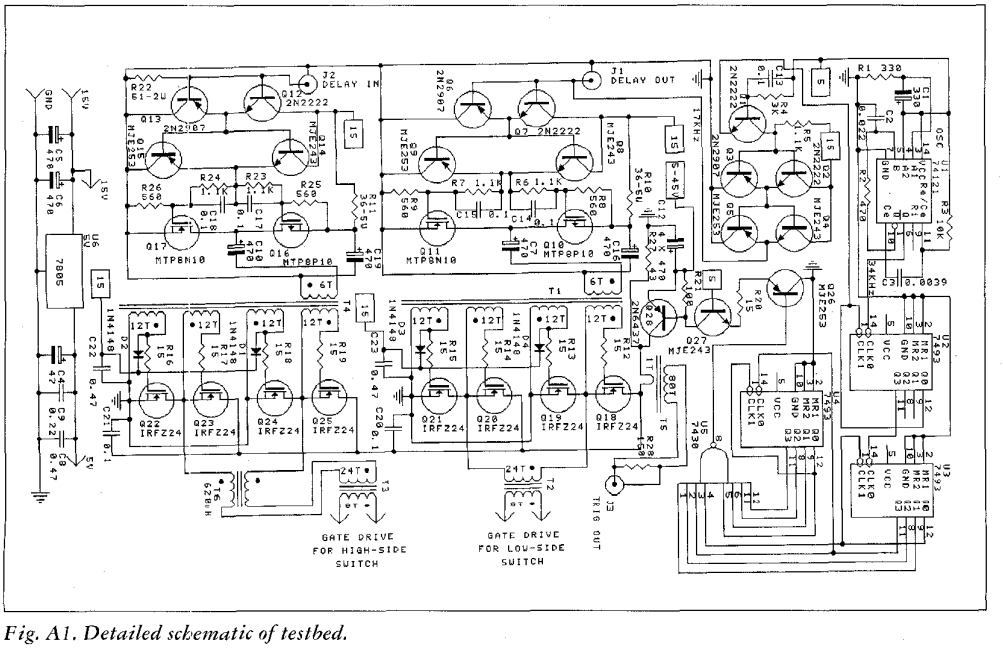

Fig. A1. Detailed schematic of testbed.

The turn-on of the enabling power results in a large current pulse through Q28 as bypass capacitors C20 and C21 are charged. This pulse provides a scope trigger output via the current-to-voltage transformer T5, which was made with a Philips 204XT250-3E2A core. An important advantage of this current transformer scheme for triggering is that it eliminates ground loop problems between the trigger ground and the power ground for the switching IGBTs. The measured waveforms taken from the IGBTs are made substantially cleaner by eliminating this ground loop.

There are two differences between the two gate-drive amplifiers themselves. The first difference is that the polarity of the primary winding of the H-bridge drive transformer is reversed for the high-side switch IGBT driver. The second difference is that a common-mode transformer (T6) is inserted between the H-bridge driver and the gate drive transformer for the high-side driver. The purpose of this common-mode transformer is to decouple the primary-to-secondary capacitance of the gate drive transformer so that large current spikes resulting from the high dv/dt that is present at the emitter of the high-side switch IGBT are not coupled to ground through the high-side switch driver. T6 was made with 15 turns of a twisted pair on a Philips 846XT250-3E2A core. The twisted pair keeps the differential inductance of this transformer low so as not to compromise the speed of the gate drive.

Winding techniques for gate drive transformers T2 and T3, and also for H-bridge driver transformers T1 and T4, determine the speed and performance of the IGBT shoot-through testbed. In order to accurately verify IGBT models of switching operations, it is important to have fast and clean gate transitions with sufficient power so that the IGBT input capacitive loading can be made to have minimal effect on the transformer output waveforms when a variety of series gate resistors are used. The gate drive transformers T2 and T3 were wound on Philips 3622PLOO-3F3 pot cores. An interleaved winding structure was used starting with a 24-turn primary made with two parallel strands of #32 magnet wire. An insulating tape layer was applied. A secondary layer was added using eight turns of five parallel strands of #32 wire, followed by another insulating tape layer. Additional similarly wound layers alternating primary and secondary were applied for a total of four primary layers and three secondary layers. All of the wire ends were sorted into their appropriate groups and tied together for the transformer leads. The leakage inductance on the primary was measured to be 0.65 μH with the secondary leads shorted together two cm from where they leave the body of the transformer. The primary-to-secondary capacitance was measured to be 370 pF.

A similar construction technique was used for the H-bridge driver transformers T1 and T4. These were wound of Philips 2616PLOO-3B7 pot cores with three primary layers interleaved with two secondary layers. Six turns of eight parallel #32 wire made each primary layer, while 12 turns of four parallel #32 wire made each secondary layer. The four parallel wires on the secondary were kept separate to become the four individual gate windings needed by the H-bridge MOSFETs. Secondary gate windings were paired with similar secondary gate windings from the second layer of secondary windings so that each MOSFET in the H-bridge was driven with two paralleled windings. Insulating tape was applied between primary and secondary layers, but not between the individual secondaries in a given layer. This construction provides not only tight coupling between primary and secondary but also between the individual gate windings as well. Diodes D1-D4 take advantage of this tight coupling to provide good gate-voltage clamping, as without the clamping slower H-bridge drive would have to be used to avoid excessive voltage ringing overshoot on the MOSFET gates. The leakage inductance measured on the primary with one secondary shorted was found to be 30 nH, and the leakage inductance measured on one secondary winding with only one other secondary winding shorted was found to be 200 nH. It should be noted that these are typical numbers as there are substantial differences in these numbers for different secondary windings due to their relative proximity to one another.

The H-bridge gate drive for the IGBTs operates from a voltage that is nominally set to 45 V in order to drive the IGBTs with a 15 V turn-on drive. This separate supply voltage was chosen to more fully utilize the MOSFETs in the H-bridge, and also to allow this voltage to be adjusted for lower IGBT gate drive voltages if desired.